Parallel Phase Shifted Carrier Pulse Width Modulation (PSCPWM) – A Novel Approach to Switching Power Amplifier Design

Preprint 4447 (G5)

Karsten Nielsen
Bang & Olufsen, Denmark
Institute of Automation, Technical University of Denmark

Presented at the 102nd Convention 1997 March 22–25 Munich, Germany

AES

AN AUDIO ENGINEERING SOCIETY PREPRINT

Parallel Phase Shifted Carrier Pulse Width Modulation (PSCPWM) - A novel approach to switching power amplifier design

Karsten Nielsen

Bang & Olufsen, Denmark
and
Institute of Automation, Technical University of Denmark

E-mail: kn@iau.dtu.dk
Internet: http:/www.iau.dtu.dk/~kn

Abstract

A new family of modulator and power stage structures for switching power amplifier systems are presented. The new modulation principle is called Phase Shifted Carrier Pulse Width Modulation (PSCPWM), which synthesizes a multiple-level pulse width modulated waveform from a single or two supply levels. This reduces the high frequency (HF) content of the pulse modulated signal, and further increases the apparent sampling frequency by a controllable integer factor N. The effective elimination of high frequency content leads to hitherto unknown possibilities in terms of possible frequency ratios (bandwidth/switching frequency), power handling capability and the design of control systems. It is shown that PSCPWM can be synthesized by using multiple push-pull switching legs in parallel, controlled by phase shifted carrier or/and phase shifted signal waveforms. A thorough theoretical analysis for Parallel Phase Shifted Carrier PWM modulation (PSCPWM) is given, based on a double Fourier series representation of the multiple level pulse width modulated waveform. Practical issues regarding PSCPWM implementation are discussed, and illustrated by example.

1. Introduction

Switching (class D) power amplifiers have numerous apparent advantages, as the combination of high efficiency, high linearity and low complexity that can be realized [8], [9], [10]. Three level double sided modulation has proven some obvious advantages over two level modulation [10]. The question arises if it is possible, by simple means, to synthesize even more efficient PWM waveforms than double-sided three level PWM, i.e. a PWM waveform that is closer to the modulating signal and has a minimal high frequency content. One approach is a scheme known as multiple-level PWM used in recent (rather complex) high power switching inverter systems [6], [7]. These recently presented multiple-level PWM switching converters are based on the use of numerous power

supply voltage levels and complex control circuitry. Furthermore, such an approach would introduce severe *distortion* from diode forward voltages. So, for a multiple-level PWM scheme to be interesting, the following requirements should hold:

- There are simple implementation strategies.
- There is a possibility for single or dual supply operation for minimal power supply complexity.
- The power stage has a high linearity, as it is the case with the H-bridge based two and threhe level modulation schemes. No extra (distorting) diodes should be required, as is the case with traditional multiple supply level based multiple level PWM systems.

The topologies presented in this paper realizing Phase Shifted Carrier Pulse Width Modulation (PSCPWM) obey all of these requirements, and it is furthermore shown that several other advantages arise by using this principle of modulation. The aim of this paper is to present these new possibilities, but also to outline the limitations.

2. General topology

The PSCPWM topology is shown in its most general form in Fig. 1. A typical approach to obtain higher powers in a switching power stage, is to parallel switches or bridge legs. By applying controlled phase shifts on either the carrier and/or the modulating signal to each switching leg, instead of just paralleling similar controlled switching legs, it is possible to synthesize highly interesting multiple-level modulation waveforms. It is of course questionable to call a multiple-level pulse train a pulse *width* modulated signal, since there is obviously also a pulse *amplitude* modulation taking place. This amplitude modulation increases with N. However, three-level PWM which contains simple amplitude modulation is known as a pulse width modulation scheme. It will also be shown that PSCPWM can be considered as a *generalization* of the traditional pulse width modulation principles, and it is therefore found appropriate to keep this designation.

3. Analysis methodology

A general theoretical treatment of PSCPWM is carried by using a double Fourier series [1], [2], [10]. Since the pulse modulated waveform in effect is obtained by superposing well known modulation waveforms, superposition can accordingly be used to obtain a general compact double Fourier series expression for PSCPWM, which allows for a high detail analysis of the spectral characteristics.

Fig. 2 illustrates a circuit equivalent for PSCPWM, where N bridge legs are paralleled. The contribution of each generator to the idle output voltage $v_{th}(t)$ can be expressed by the voltage division factor:

$$K = \frac{\frac{sL}{N-1}}{sL + \frac{sL}{N-1}} \tag{1}$$

Thus, $v_{th}(t)$ can be written as:

$$v_{th}(t) = K(v_1(t)+\ldots v_N(t)) = \frac{v_1(t)+\ldots v_N(t)}{N} \tag{2}$$

The short circuit current $i_{sc}(t)$ and Thevenin impedance Z_{th} are:

$$i_{sc}(t) = \frac{v_1(t)+\ldots+v_N(t)}{sL} \tag{3}$$

$$Z_{th} = \frac{v_{th}(t)}{i_{sc}(t)} = \frac{sL}{N} \tag{4}$$

From this model it is clear, that normal paralleling of N switching legs causes the resulting output $v(t)$ to have the *same* modulation characteristics as each individual leg. The only gain by such paralleling of identical bridge legs is therefore a higher current handling capability.

3.1 Derivation of double Fourier series for double sided PSCPWM

As it is the case with two and three level modulation schemes, PSCPWM can of course be based on both a single sided and a double sided reference. The systematic analysis of all modulation variants in [10] illustrated the superior performance of double sided modulation, and the following will therefore be concentrated on double sided modulation. A similar expression can of course be developed for single sided modulation, by following the same procedure as below for double sided modulation. The analysis is based on the use of Natural sampled - AD - Double sided modulation NADD [10] in each switching leg:

$$\begin{aligned} F_{NADD}(t) = {} & M\cos(y) \\ & + 2\sum_{m=1}^{\infty} \frac{J_0(m\pi\frac{M}{2})}{\frac{m\pi}{2}} \sin(\frac{m\pi}{2})\cos(mx) \\ & + 2\sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\infty} \frac{J_n(m\pi\frac{M}{2})}{\frac{m\pi}{2}} \sin(\frac{(m+n)\pi}{2})\cos(mx+ny)t \end{aligned} \tag{5}$$

Where:

M	Modulation index. $M \in [0;1]$.
$x=\omega_c t$	ω_c = Audio signal angle frequency.
$y=\omega t$	ω = Carrier signal angle frequency.
J_n	Bessel function of nth order.
n	Index to the harmonics of the audio signal.
m	Index to the harmonics of the carrier signal.

The double Fourier series of NADD with a phase shifted carrier is obtained by the following substitution

$$x - \theta \rightarrow x \tag{6}$$

in the expression for NADD:

$$\begin{aligned} F_{NADD,\theta}(t) = {} & M\cos(y) \\ & + 2\sum_{m=1}^{\infty} \frac{J_0(m\pi\frac{M}{2})}{\frac{m\pi}{2}} \sin(\frac{m\pi}{2})\cos(mx - m\theta) \\ & + 2\sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\infty} \frac{J_n(m\pi\frac{M}{2})}{\frac{m\pi}{2}} \sin(\frac{(m+n)\pi}{2})\cos(mx + ny - m\theta) \end{aligned} \tag{7}$$

Applying the same modulating signals to all legs causes the Fourier series for the equivalent Thevenin generator to be equal to the Fourier series for NADD, and there is therefore no direct advantage of this approach besides the lower current handling capability in each switching leg. The following derivations will show, that the bridge legs should indeed *not* just be paralleled. A much more attractive control scheme is obtained by the following successive phase shifts of the carrier waveform :

$$\theta_p = (p-1)\frac{2\pi}{N}, p \in \{0; N-1\} \tag{8}$$

The double Fourier series expansion for each of the generator output voltages gets :

$$
\begin{aligned}
F_{NADD,\theta_p}(t) = {} & M\cos(y) \\
& + 2\sum_{m=1}^{\infty} \frac{J_0(m\pi\frac{M}{2})}{\frac{m\pi}{2}} \sin(\frac{m\pi}{2})\cos(mx - m(p-1)\frac{2\pi}{N}) \\
& + 2\sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\infty} \frac{J_n(m\pi\frac{M}{2})}{\frac{m\pi}{2}} \sin(\frac{(m+n)\pi}{2})\cos(mx + ny - m(p-1)\frac{2\pi}{N})
\end{aligned}
\tag{9}
$$

The equivalent generator voltage of the modulator and power stage for N paralleled switching legs can be written as (2) :

$$
F_{NADD,N}(t) = \frac{1}{N}\sum_{p=1}^{N} F_{NADD,\theta_p}(t) \tag{10}
$$

From (8), (9) and (10) the series for $F_{NADD,N}(t)$ can be found :

$$
\begin{aligned}
F_{NADD,N}(t) = {} & M\cos(y) \\
& + \frac{2}{N}\sum_{m=1}^{\infty} \frac{J_0(m\pi\frac{M}{2})}{m\pi} \sin(\frac{m\pi}{2}) \cdot \\
& \left[\cos(mx) + \cos(mx - m\frac{2\pi}{N}) + \cdots + \cos(mx - m(N-1)\frac{2\pi}{N})\right] \\
& + \frac{2}{N}\sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\infty} \frac{J_n(m\pi\frac{M}{2})}{\frac{m\pi}{2}} \sin(\frac{(m+n)\pi}{2}) \cdot \\
& \left[\cos(mx + ny) + \cos(mx + ny - m\frac{2\pi}{N}) + \cdots + \cos(mx + ny - m(N-1)\frac{2\pi}{N})\right]
\end{aligned}
\tag{11}
$$

Since:

$$
\frac{1}{N}\sum_{p=1}^{N} \cos(x - m(p-1)\frac{2\pi}{N}) = \begin{cases} \cos(x) & for\ m \in \{N, 2N, 3N, \cdots\} \\ 0 & else \end{cases} \tag{12}
$$

(11) is be reduced to:

$$F_{NADD,N}(t) = M\cos(y) + 2\sum_{m\in\{N,2N,3N,\cdots\}} \frac{J_0(m\pi\frac{M}{2})}{\frac{m\pi}{2}} \sin(\frac{m\pi}{2})\cos(mx) + 2\sum_{m\in\{N,2N,3N,\cdots\}}\sum_{n=\pm1}^{\infty} \frac{J_n(m\pi\frac{M}{2})}{\frac{m\pi}{2}} \sin(\frac{(m+n)\pi}{2})\cos(mx+ny) \quad (13)$$

A detailed investigation of (13) reveals some very interesting characteristics for PSCPWM :

- The spectrum only contains components around multiples of $N\omega_c$!. Thus, PSCPWM provides an *effective* increase in sampling frequency by a factor of *N*. This effective increase of sampling frequency is highly interesting, since it can be used effectively to reduce the switching frequency in each switching leg.
- With odd order PSCPWM the second term in the series is zero, and *no* harmonics of the carrier are therefore present in the spectrum. This causes the modulated output to be totally free from components at idle.

4. Simulation

In this section the interesting characteristics of PSCPWM are illustrated in both time- and frequency domain.

Fig. 3 - Fig. 7 illustrates the general principles of PSCPWM in the time domain for different N. The chosen parameter values are:

- Frequency ratio : q=1/16.
- Modulation index: M=0dB and M=-20dB. The two modulation indexes are chosen to illustrate the characteristics full modulation and at 'lower' modulation depth, which is specially interesting with higher N.
- Number of levels: N={2,3,4,5,9]. N=2 and N=3 illustrate, how PSCPWM can be considered a *generalization* of the traditional two- and three-level modulation schemes. N=4 and N=5 illustrate the (for switching power amplifier applications) most interesting PSCPWM methods, given the fact that a reasonably low modulator and power stage complexity is desired. N=9 is not practically interesting but illustrate how it is possible in principle to totally eliminate the modulation components. Thus, with N=∞ PSCPWM provides a *perfect synthesis* of the modulating wave and *no* other components whatsoever.

The structure of the time domain illustrations in Fig. 3 - Fig. 7 is the same for all N. Top figure: Modulating signal and the carrier waveforms necessary to

synthesize the resulting PWM waveform. Bottom figure: The effective pulse modulated signal feed to demodulation in the filter.

Fig. 8 - Fig. 12 illustrates the frequency spectra for the considered parameter set. For all N, the following is illustrated:

- The worst case amplitude spectrum, corresponding to M=0dB.
- A Harmonic Envelope Surface (HES) as defined in [10], illustrating the spectral amplitude characteristics at all modulation indexes in the range -100 dB to 0dB. The amplitude is shown as a grayscale, as defined left in the figure by the fundamental of the modulating wave, i.e. white indicates 0dB amplitude and black indicates that the components are damped at least 100dB relative to full scale.

All spectra are shown up to f = 9 (normalized to the carrier frequency). In the following sections, the time and frequency domain characteristics for each distinct PSCPWM method is discussed.

4.1 Two-level PSCPWM (N=1)

2-level PSCPWM corresponds to the traditional double sided two level modulation (NADD) [10]. The HES-plot clearly illustrates the 'crowded' HF-spectrum, with components around each multiple of the carrier frequency.

4.2 3-level PSCPWM (N=2)

3-level PSCPWM synthesizes the exact same PWM waveform as double sided three level modulation (NBDD) [10]. This is obvious form the HES-plot in Fig. 9. 3-level PSCPWM can therefore be seen as an alternative implementation strategy of NBDD, where the carrier is shifted instead of the signal as it is the case in the general implementation of 3-level modulation.

4.3 4-level PSCPWM (N=3)

The time domain analysis of (Fig. 5) illustrates how the resulting pulse waveform already at N=3 become closer to the modulating sine wave. The switch component amplitude is obviously reduced in amplitude by a factor of 3 compared to NADD. Switching components remains present in the output at lower output levels. At idle, a square will be present with a normalized amplitude of 1/3. This is similar to two level modulation, and it is a *general characteristic of even-level* PSCPWM. Note form the HES-plot for 4-level PSCPWM in comparison to 3-level and 2-level PSCPWM, that what has actually happened is an elimination of the components that are not harmonics of N, as directly seen from the general double Fourier series in (13).

4.4 5-level PSCPWM (N=4)

The time (Fig. 6) and frequency domain (Fig. 11) analysis of 5-level PSCPWM illustrate the effective increase in sampling frequency by a factor of N (four).

Also note the interesting characteristics at lower output levels, where the HF content diminish totally. This general characteristic of *odd level* PSCPWM is most obvious form the HES-plot, which is totally black near idle operation (M=-100dB).

4.5 9-level PSCPWM (N=8)

The simulation of 9-level PWM (Fig. 7 and Fig. 12) illustrates how a *near perfect* synthesis of the modulating sine wave can be carried out by PSCPWM. However, the synthesis of the 9 levels requires 8 parallel coupled half bridges and 8 inductors and is therefore mainly of theoretical interest.

5. Circuit topologies

As it is apparent form the general circuit topology in Fig. 1, more output switches are required than for the two- and three-level modulation schemes. However, this is to some degree compensated by the lower current requirements in each of the switches. In terms of silicon area there are no real difference, i.e the 8 transistors required in a 5-level PSCPWM circuit could actually be the four transistors in a bridge circuit, where each transistor die is divided in half.

5.1 Even level PSCPWM circuit topology

The circuit topology for efficient realization of even level PSCPWM is illustrated by the 4-level circuit in Fig. 14 (power stage) and Fig. 15 (modulator structure). A dual rail supply is necessary in order to provide a DC free output. Practical near lossless superposition of half-bridge generator voltages is realized by inductors. A requirement for perfect synthesis of the resulting output voltage is therefore, that the inductors are exactly equal. The summing inductors in combination with the capacitance C form an effective 2. order attenuation of the switching components. Due to the effective N-factor increase in sampling frequency by PSCPWM, this simple second order filter, in combination with the inherent low high frequency content, will provide near *perfect demodulation* with typical bandwidth/carrier frequency ratios.

5.2 Odd level PSCPWM circuit topology (balanced PSCPWM)

Odd level PSCPWM could of course be synthesized by the same circuit topology as even level PSCPWM. However, an alternative and better topology has been developed, which proves to be advantageous. The basic idea is to use a 'balanced' drive of the two terminal load, as illustrated by the 5-level circuit in Fig. 14 (power stage) and Fig. 16 (modulator structure). This balanced PSCPWM topology provides several advantages:

- Only a single supply level is required, independent on the number of levels that need to be synthesized.
- The breakdown voltage requirement to each of the transistors is *halved*. This is very important, since the paracitic components (e.g. capacitances) of the switching transistors depend heavily on the breakdown voltage.

The 'balanced drive' has the disadvantage of generating common-mode components over the load terminals.

5.3 Practical modulator implementation

The modulator could be implemented in both analog and digital domain. Phase shifted carriers could be realized by a higher frequency clock, generating phase shifted square waves at the desired carrier frequency for each half-bridge. The phase shifted carriers can thereafter simply be obtained by integrating the phase-shifted square waves. Fig. 15 and Fig. 16 illustrates the implementation of both the 4-level and 5-level analog PSCPWM modulator. Note the inversion of the modulating signal in the 5-level modulator, which is necessary due to the 'balanced' drive. The analog implementation of the modulators is seen to be reasonably simple.

6. Simulation of a practical example

In this section, a more practical example is analyzed. Consider the implementation of a high power amplifier with the following general specifications :

- 500W continuos output power.
- Bandwidth: 20Hz-20KHz.
- 4 ohm nomial load impedance.

An implementation using 4-level PSCPWM is considered. The switching frequency is set as low as 125KHz in each switching leg. The filter components are L=35μH and C=722nH (Bessel filter). Fig 17 shows the effective differential load voltage, and the demodulated version. It is clear that the simple second order filtering provides good demodulation, even though the each leg switches with only 125KHz. Similar simulations have been carried out for 5-level PSCPWM (not shown). The simulations indicate, that the switching frequency in each leg could be further reduced to 80-100KHz. Furthermore, the requirements for breakdown voltage is reduced form 140V to 70V, meaning that standard 100V low current FET's are perfectly usable, despite the high total power handling capability of the power stage.

The table below compares essential parameters for four different modulation schemes in order to illustrate the possibilities of PSCPWM:

- 2-level PWM (NADD).
- 3-level PWM (NBDD).
- 4-level PSCPWM.
- 5-level PSCPWM.

Parameter	NADD (2-level)	NBDD (3-level)	4-level PSCPWM	5-level PSCPWM
N	1	2	3	4
Num. of FET's	2/4	4	6	8
FET breakdown voltage	140V/70V	70V	140V	70V
Switching frequency	250KHz	250KHz	125KHz	100KHz
Max. IM harm. ampl.	~ 0dB	~ -12dB	~ -16dB	~ -20dB

The results illustrate the beneficial characteristics of PSCPWM in terms of switching frequency in each switching leg and implicit lower maximal amplitude of the high frequency components.

7. Conclusions

A new family of modulator and power stage structures for switching power amplifier systems have been presented, in combination with a multiple-level modulation scheme, Phase Shifted Carrier PWM modulation (PSCPWM). A detailed analyses has been carried out based on the derivation of a double Fourier series for the general PSCPWM principle. It has been shown, that PSCPWM can be considered a generalization of the known two- and three-level modulation schemes. The general advantages of PSCPWM over the traditional two or three level based modulation schemes are concluded to be:

- PSCPWM synthesizes a pulse modulated wave which is much closer to the modulation signal (sine wave). The benefit is a dramatically reduced HF amplitude spectrum, which is beneficial in terms of both demodulation and when designing control systems.
- PSCPWM provides an N-factor increase in the *effective* sampling frequency. This lowers the switching frequencies in each switching leg.

Although the general possibilities of PSCPWM are highly exciting, it is important to emphasize the factors that need care in order not to be limiting factors:

- The number of inductors increase with *N*. Furthermore the inductances need to be reasonably identical for the harmonic cancellation.
- The complexity added by multiple precision phase shifted carriers. This added complexity will in general not dominate over the power stage and this is therefore less important.
- The parallelling of PWM generators means that circulating current can flow between the PWM legs. This should be prevented.

These issues do *not* cause harmonic distortion, but only influence the HF-spectral characteristics and the efficiency. An area for future research is a systematic investigation of the sensitivity of the harmonic cancellation to phase shift accuracy and inductor tolerances. Such investigations could be carried out on the basis of the presented analytical double Fourier series expressions for PSCPWM.

8. Acknowledgments

The author is grateful to professor John Vanderkooy, University of Waterloo, Canada for his comments on this and the parallel paper [10]. John Vanderkooy also deserves credit for inspiring the author to research in new PWM methods. Furthermore, the author wishes to thank Bang&Olufsen, the Danish Energy Agency and CETEC for their economic/technical support in the research project.

9. References

[1] Bennett, W.R.
" New Results in the Calculation of Modulation Products "
Bell system Technical Journal. 1933. pp. 228-243.

[2] Black, H.S.
Modulation Theory
Van Nostrand Company, 1953.

[3] Bowes, S.R. et al.
"Novel approach to the analysis and syntesis of modulation processes in power converters"
Proc. IEE, Vol. 122, No. 5, May 1975.

[4] Attwood, B.E
" Design Parameters Important for the Optimization of Very-High-Fidelity PWM (Class D) Audio Amplifiers "
JAES. Vol. 31. No. 11. Nov. 1983.

[5] Sethuraman, S.K. et al.
" PWM: A survey of modulation strategies, their spectrum analysis and microprocessor implementation ".
1987 UPEC. pp. 1-5.

[6] Rojas, R. et al.
" PWM Control Method for a four-level inverter "
IEE Proc.-Electr. Power Appl., Vol. 142, No.6, Nov. 1995. pp. 390-396.

[7] Lai, J.S. et al.
" Multilevel Converters - A New Breed of Power Converters "
IEEE Trans. on Ind. Appl., Vol. 32, No. 3, May/June 1996. pp. 509-517.

[8] Nielsen, Karsten
" High Fidelity PWM based Amplifier Concept for active speaker

systems with a very Low Energy Consumption "
100th AES Convention. Copenhagen, May 1996. Preprint 4259.

[9] Anderskouv N. , Nielsen, K. Andersen, M.
"High Fidelity Pulse Width Modulation Amplifiers based on Novel Double Loop Feedback Techniques "
100th AES Convention. Copenhagen, May 1996. Preprint 4258.

[10] Nielsen, Karsten
" A Review and Comparison of Pulse Width Modulation schemes suitable for Switching Power Amplifier systems "
To be presented at the 102th AES Convention (this convention). Munich, Germany. March 1997.

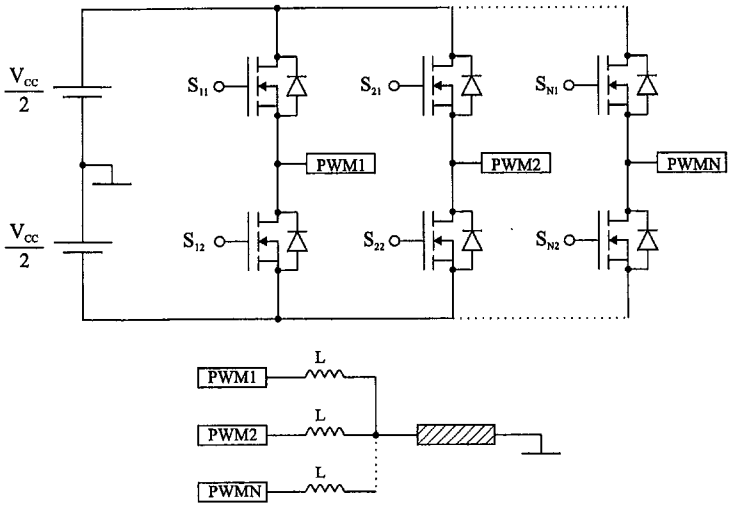


Fig. 1 General PSCPWM system, obtained by paralleling of switching legs and intelligent control.

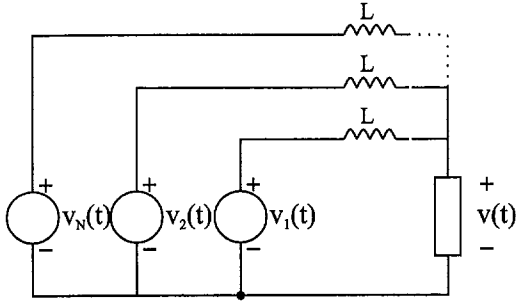


Fig. 2 PSCPWM equivalent for analytical treatment.

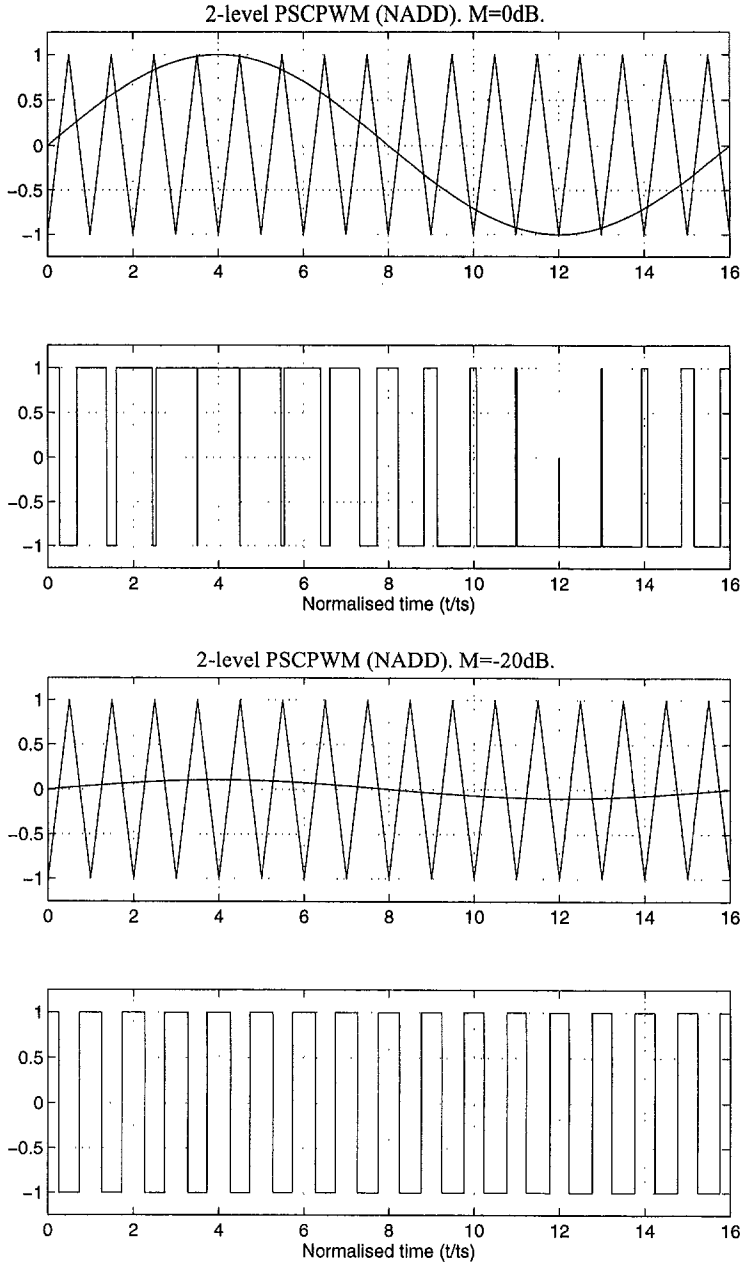


Fig. 3 Time domain analysis of NADD (2-level PSCPWM) at M=0dB and M=-20dB.

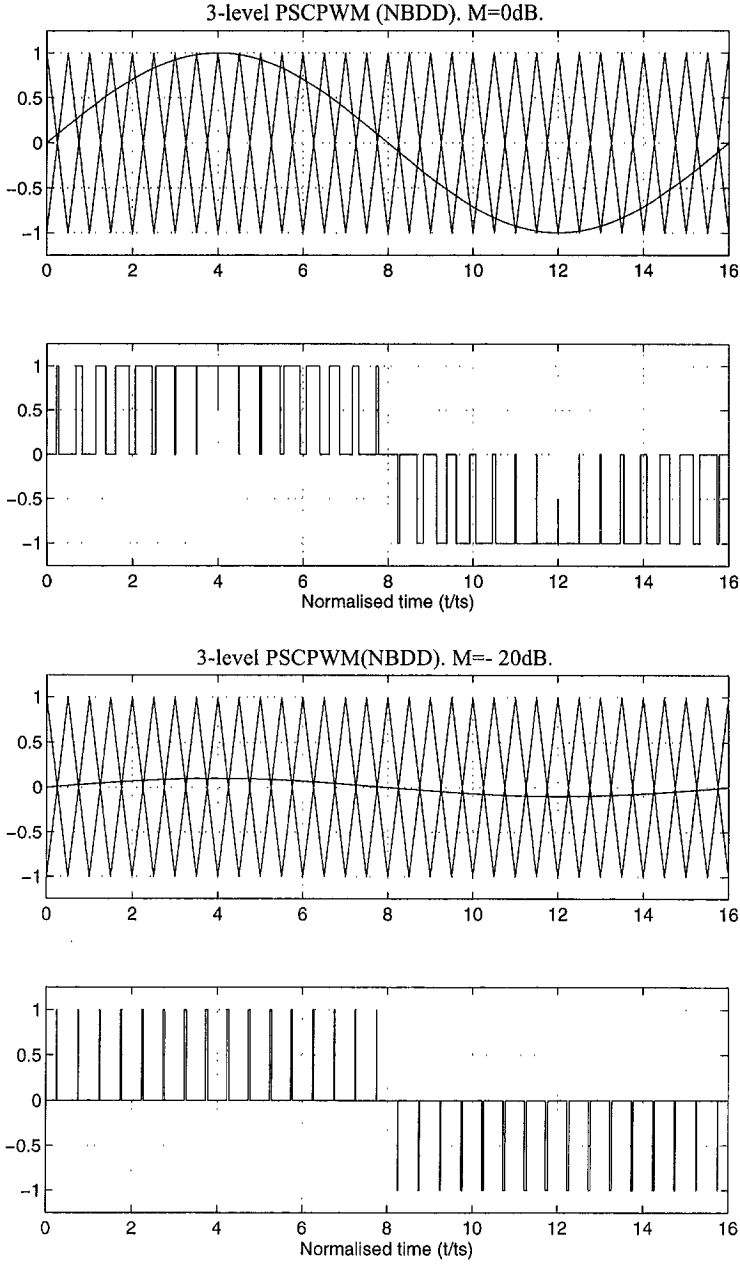


Fig. 4 Time domain analysis of NBDD (3-level PSCPWM) at M=0dB and M=-20dB.

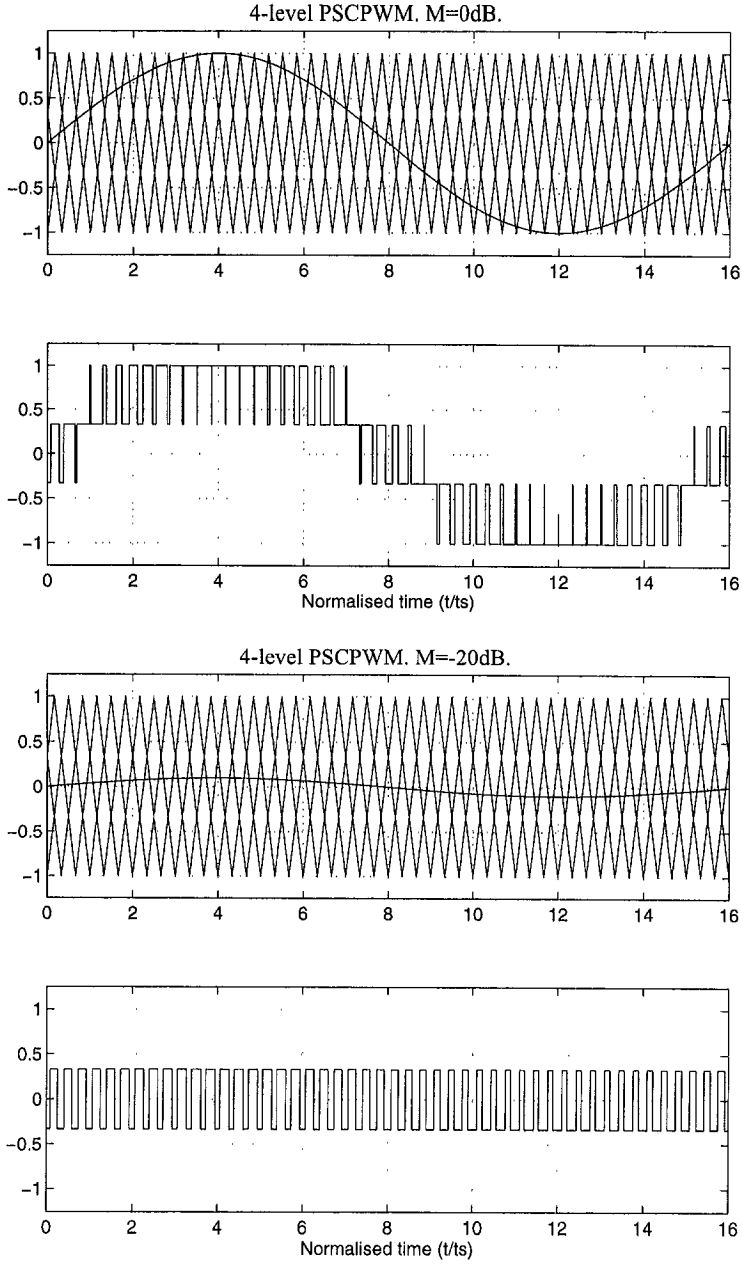


Fig. 5 Time domain analysis of 4-level PSCPWM at M=0dB and M=-20dB.

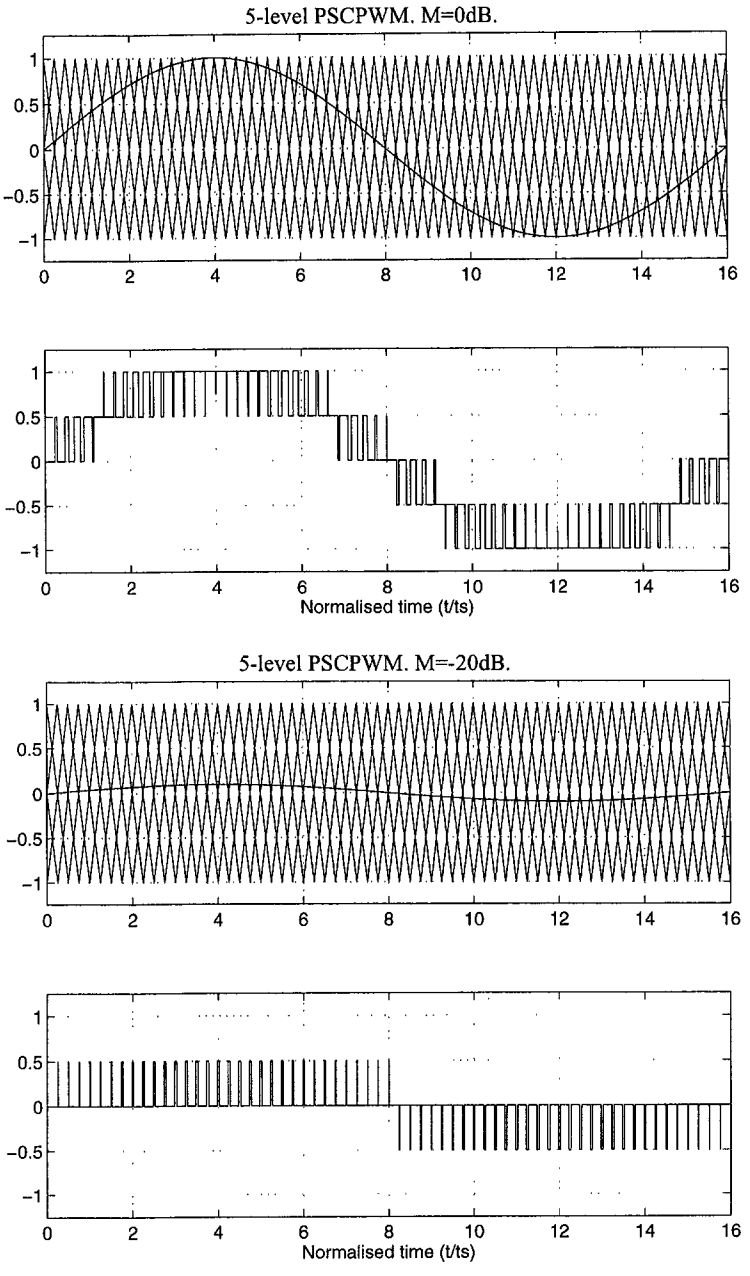


Fig. 6 Time domain analysis of 5-level PSCPWM at M=0dB and M=-20dB.

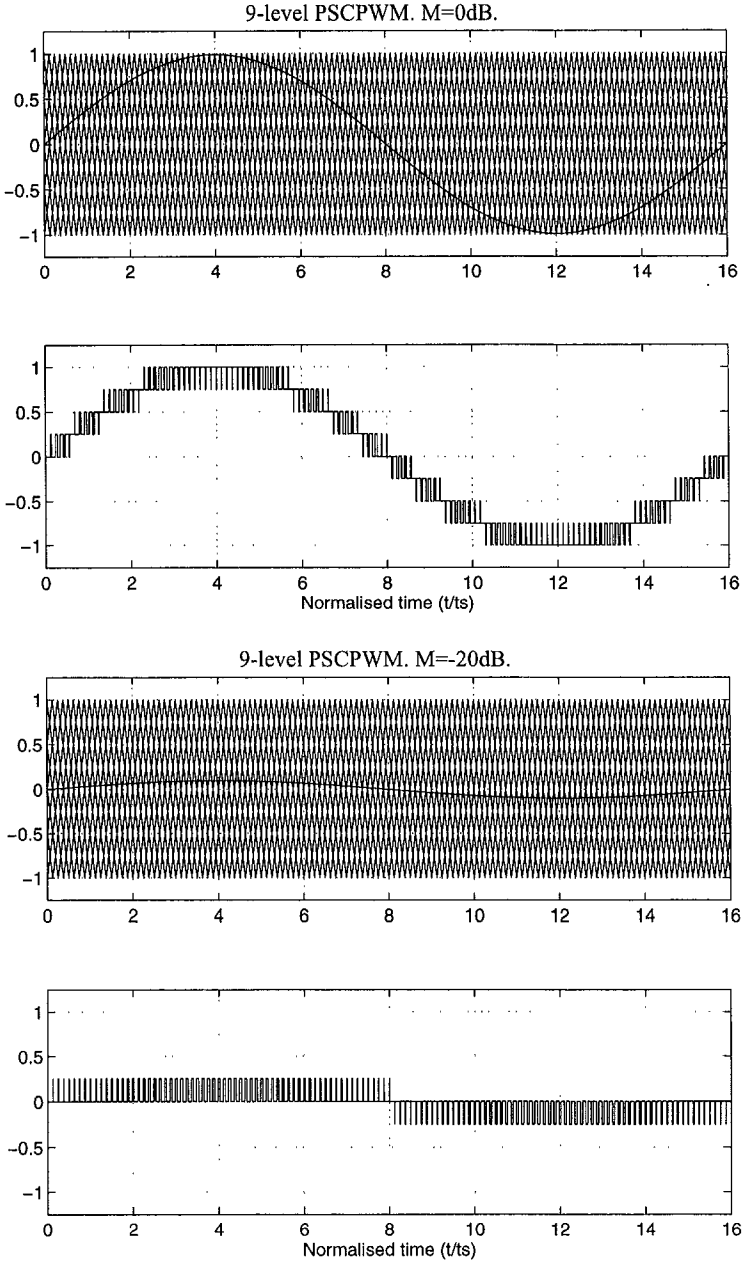


Fig. 7 Time domain analysis of 9-level PSCPWM at M=0dB and M=-20dB.

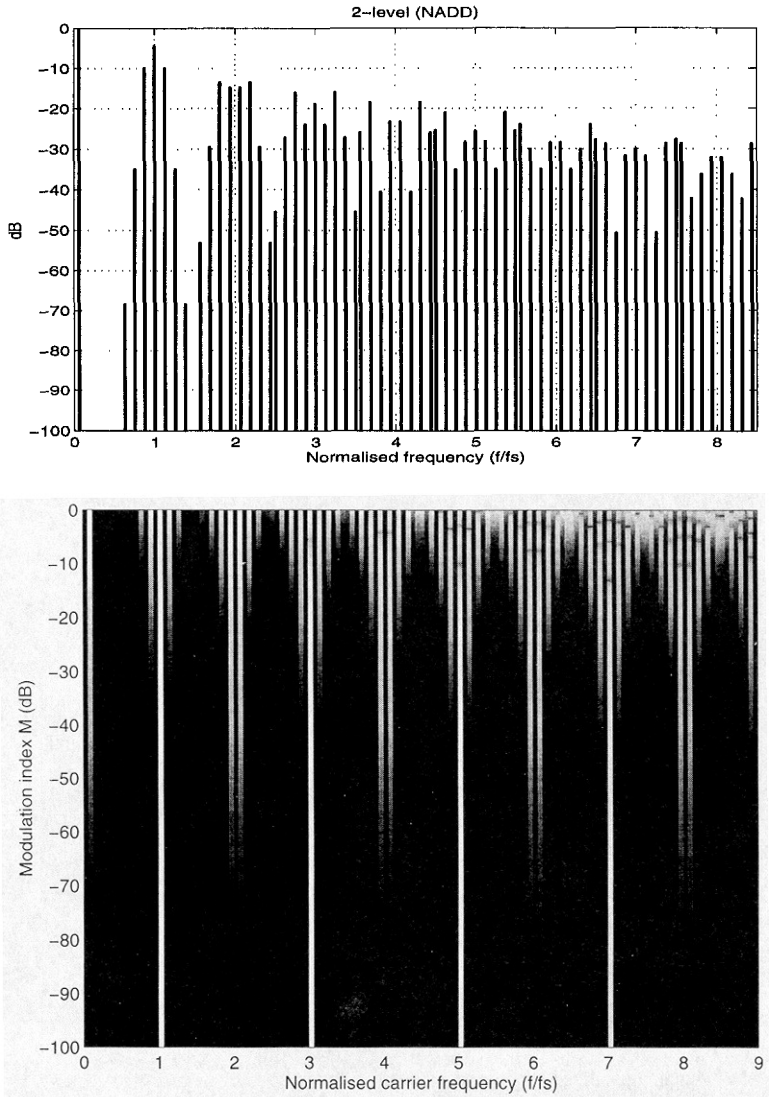


Fig. 8 Frequency domain characteristics for NADD (Natural sampled - AD - Double sided modulation), illustrated by the amplitude spectrum with a frequency ratio q=1/16, M=0dB. The bottom figure is a Harmonic Envelope Surface (HES)-plot for q=1/16.

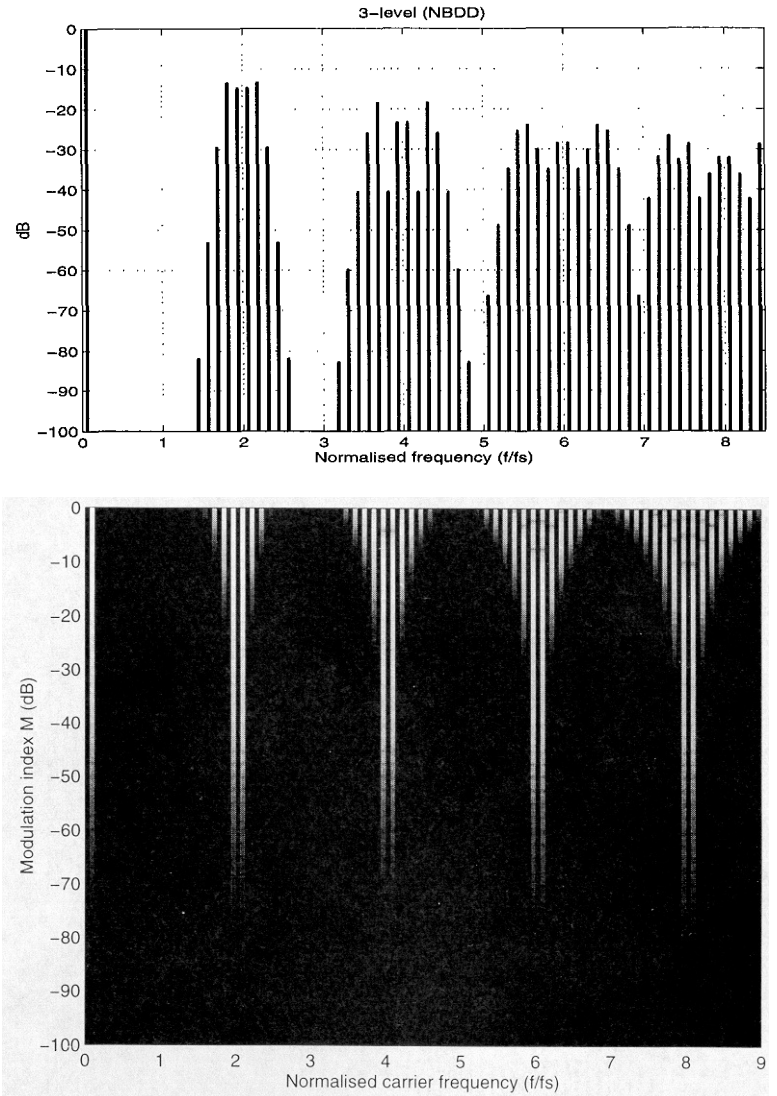


Fig. 9 Frequency domain characteristics for NBDD (Natural sampled - BD - Double sided modulation), illustrated by the amplitude spectrum with q =1/16, M=0dB. The bottom figure is a Harmonic Envelope Surface (HES)-plot for q=1/16.

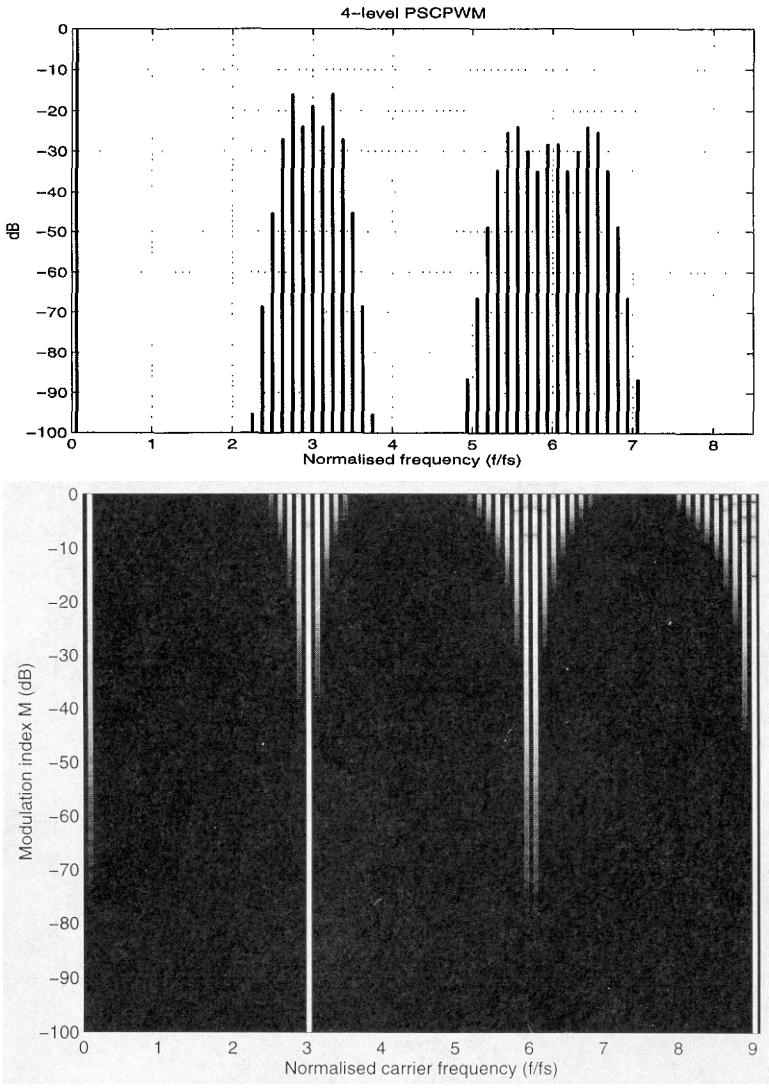


Fig. 10 Frequency domain characteristics for 4-level PSCPWM, illustrated by the amplitude spectrum with q=1/16, M=0dB. The bottom figure is a Harmonic Envelope Surface (HES)-plot for q=1/16.

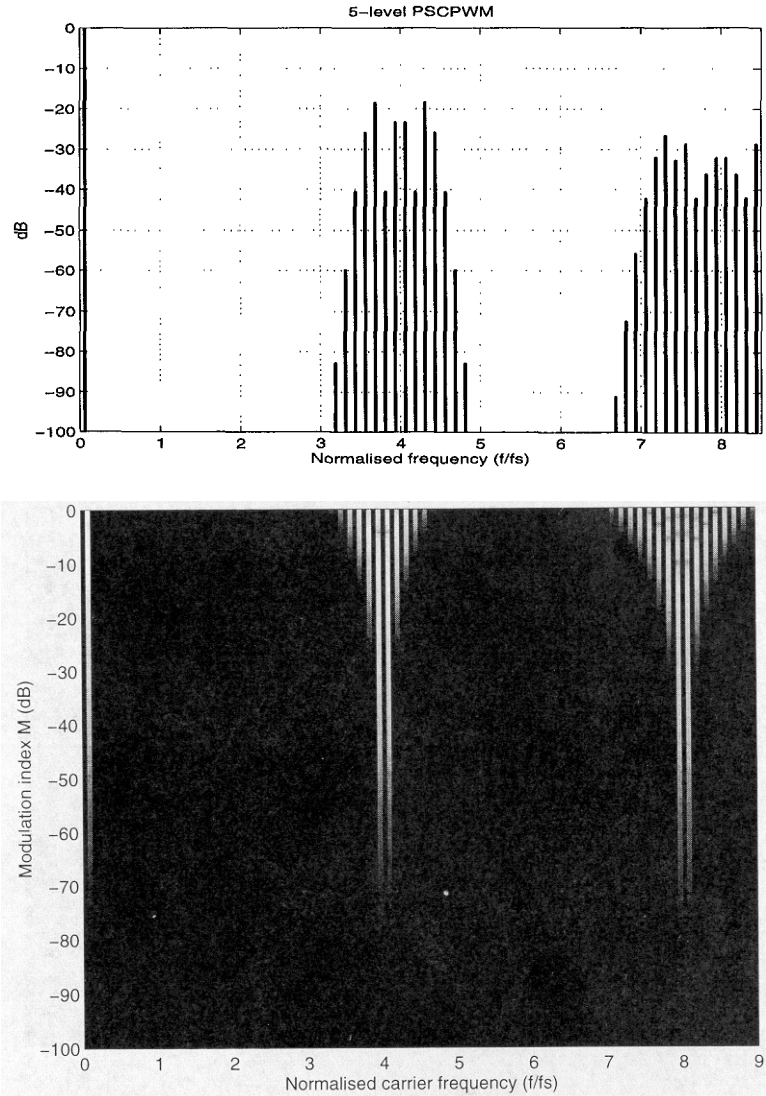


Fig. 11 Frequency domain characteristics for 5-level PSCPWM, illustrated by the amplitude spectrum with f=1/16, M=0dB. The bottom figure is a Harmonic Envelope Surface (HES)-plot for q=1/16.

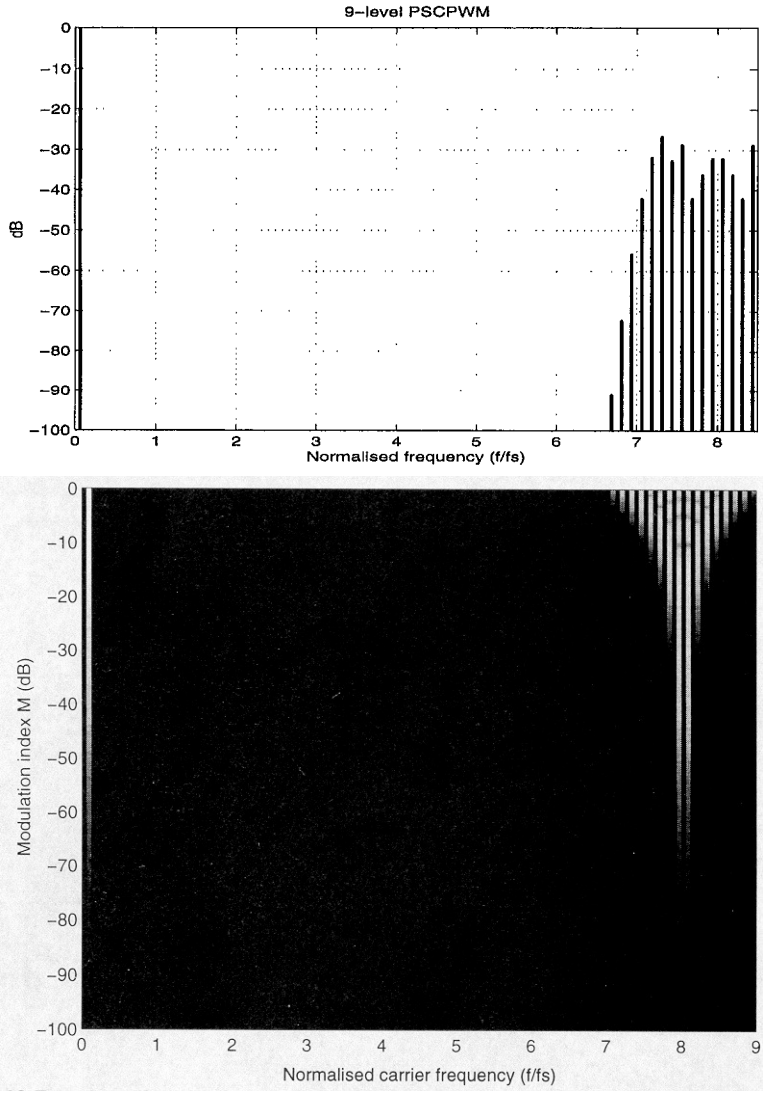


Fig. 12 Frequency domain characteristics for 9-level PSCPWM, illustrated by the amplitude spectrum with f=1/16, M=0dB. The bottom figure is a Harmonic Envelope Surface (HES)-plot for q=1/16.

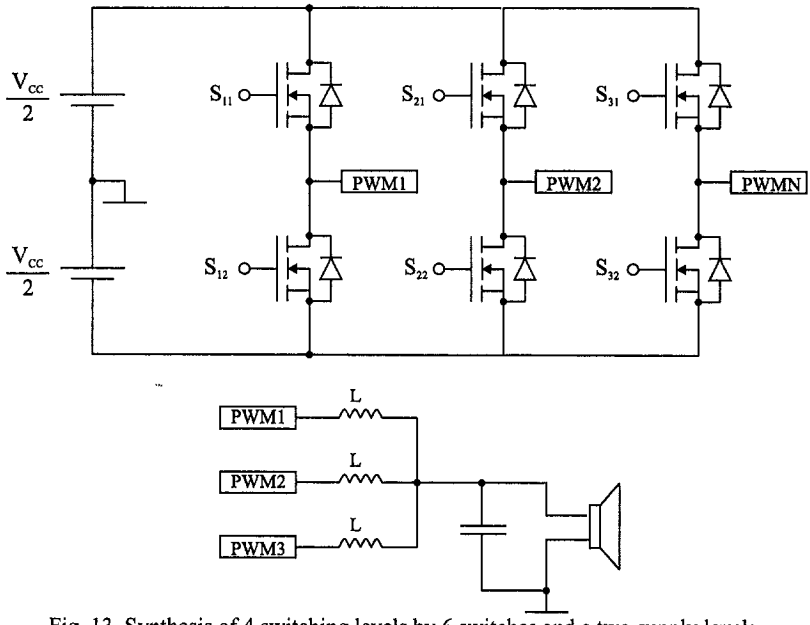
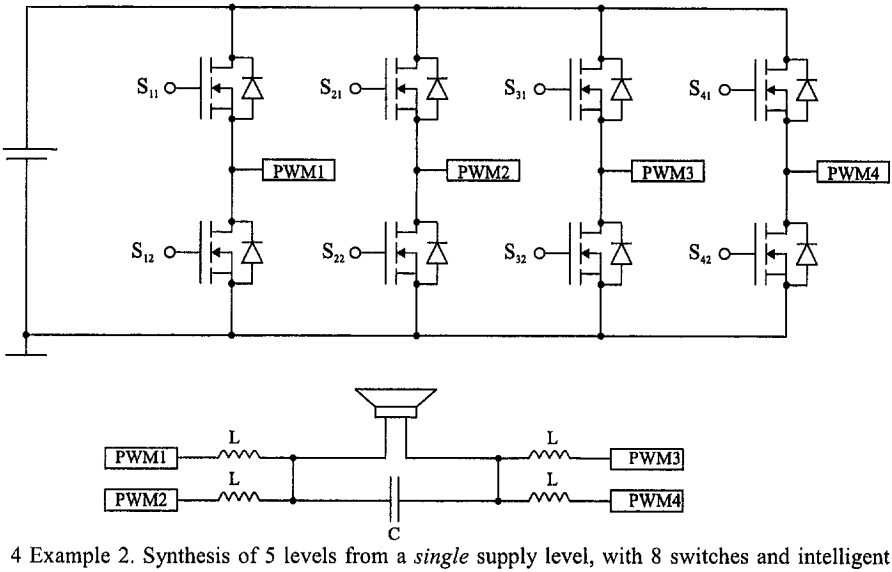


Fig. 13 Synthesis of 4 switching levels by 6 switches and a two supply levels.



4 Example 2. Synthesis of 5 levels from a *single* supply level, with 8 switches and intelligent
)l.

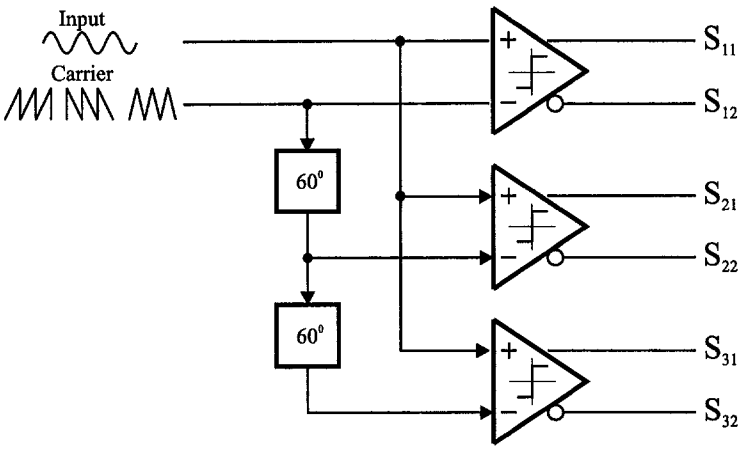


Fig. 15 4-level PSCPWM modulator structure.

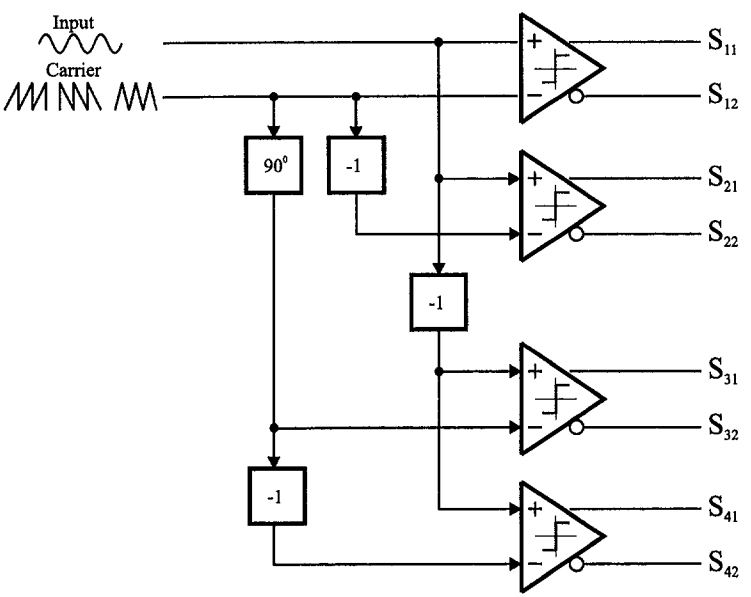


Fig. 16 5-level PSCPWM modulator structure.

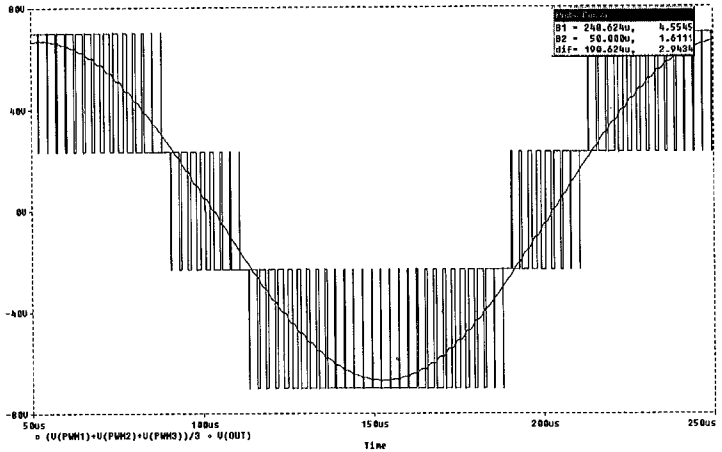


Fig 17 Essential voltages in the 500W 4-level PSCPWM power stage. A simple 2. order post filter provides near perfect demodulation despite a switching frequency of only 125KHz in each switching leg.