



Design Transition Guide – AK4490 to AK4490R/93S

- The AK4490EQ and AK4493EQ, which both came in LQFP packages, have been discontinued. The AK4490REQ and AK4493SEQ (both in LQFP packages, as well) are re-designed versions of those devices and are the recommended replacements for new and existing designs.
- The AK4490EN, which came in a QFN package, has also been discontinued. The recommended replacements are also the AK4490REQ or AK4493SEQ (both LQFP devices as noted). Re-design efforts will therefore need to address the package change, as well as reassignment of nearly all pins.

Notes on device lineage and hardware compatibility

The AK4493EQ was the successor to the AK4490EQ. Some feature updates implemented on the AK4493EQ necessitated some minor pinout and system design changes with respect to the AK4490EQ.

The AK4490REQ and AK4493SEQ are both descended from the AK4493EQ and share the same pinouts, despite slightly differing feature sets. All three feature an LDO which optionally provides the 1.8V digital supply voltage.

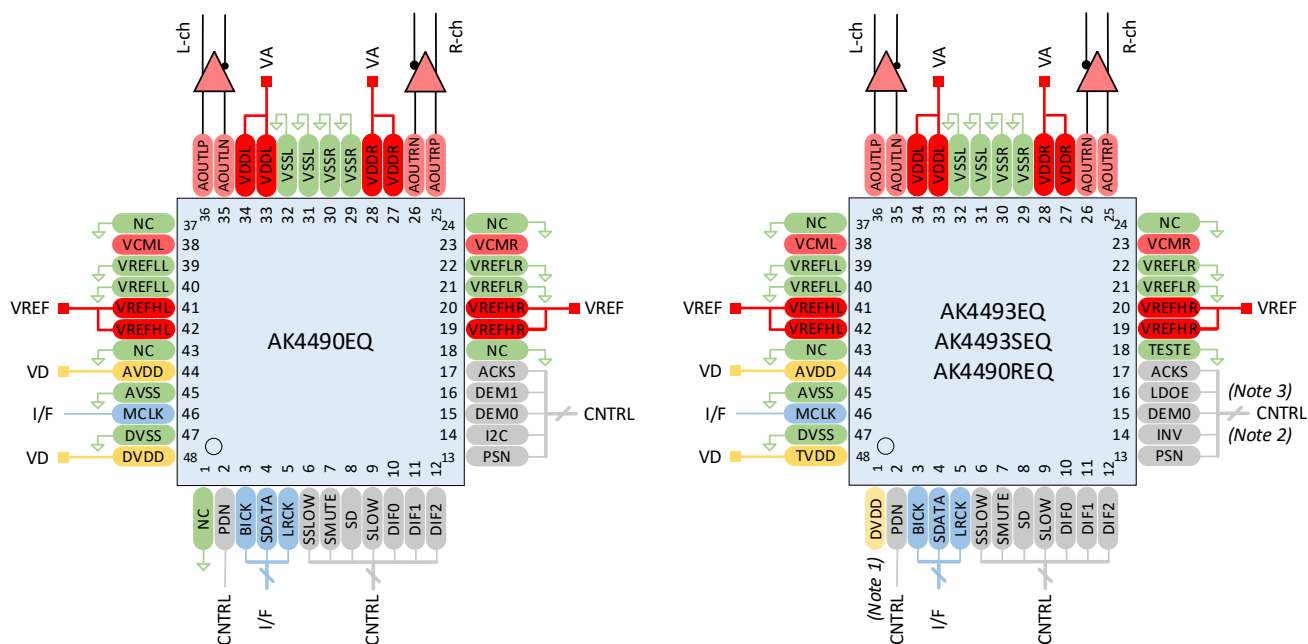
Hardware Design Transition Procedure

[EQ to EQ Transition (LQFP to LQFP)]

Transitioning from AK4490EQ to AK4490R/93S requires some minor pinout and system design changes. Pins 1 and 16 are crucial and pertain to the integrated LDO (this was not present on AK4490EQ).

Note that while the AK4490EQ supported analog and VREF supply voltages ranges of $4.75V < 5V < 7V$, the voltage range of the AK4493SEQ and AK4490REQ has been reduced to $4.75V < 5V < 5.25V$.

Figure 1 is an illustration comparing the pinout and circuit arrangements of the AK4490EQ and AK4493/93S/90R (EQ). This figure shows the abbreviated pin names for Parallel control mode; however, Serial control mode also applies.



- Notes:
- 1 - Pin 1 is DVDD (1.8V LDO output) and requires 1uF cap. to ground.
 - 2 - Pin 14 is INV and if HIGH will invert analog output polarity (Parallel mode only).
 - 3 - Pin 16 is LDOE and should be set HIGH or left open to enable 1.8V LDO.

Figure 1– Pinout and circuit arrangements of the AK4490EQ vs. AK4493/93S/90R

Refer to [Table 1](#) below for the summary of pin and system design changes transitioning from the AK4490EQ to the AK4493EQ/93SEQ/90REQ.

Table 1. Summary of changes for transitioning from AK4490EQ to AK4490R/93S (LQFP pkg. to LQFP pkg.)

Pin #	Pin name (AK4490EQ)	Pin name (AK4490R/93S)	System design impact
1	NC	DVDD (1.8V)	DVDD (1.8V) added for integrated LDO 1.8V output. Connect to added 1uF capacitor, which is to be also connected to ground.
15	DEM0*	DEM0*	*Parallel Control mode: tie HIGH if desired to disable De-emphasis; the AK4490EQ has an internal pull-up, while the AK4490R/93S does not.
16	DEM1	LDOE	Tie HIGH or leave open to enable integrated 1.8V LDO; the AK4490EQ has an internal pull-down, while the AK4490R/93S has an internal pull-up.
17	ACKS*	ACKS*	*Parallel Control mode: tie LOW to disable ACKS mode; the AK4490EQ has an internal pull-down, while the AK4490R/93S does not.
19, 20	VREFHR	VREFHR	Max. operating voltage is 5.25V.
27, 28	VDDR	VDDR	Max. operating voltage is 5.25V.
33, 34	VDDL	VDDL	Max. operating voltage is 5.25V.
41, 42	VREFHL	VREFHL	Max. operating voltage is 5.25V.
48	DVDD (3.3V)	TVDD	Inconsequential change from 3.3V (core + I/O) to 3.3V (LDO + I/O) supply voltage input.

[EN to EQ Transition (QFN to LQFP)]

Figure 2 is an illustration comparing the pinout and circuit arrangements of the AK4490EN and AK4493/93S/90R. This figure shows the example of Parallel control mode; however, Serial control mode also applies. Notice that most pins are shifted to other locations, and there are digital supply changes for the 1.8V LDO per Note 1 and Note 3.

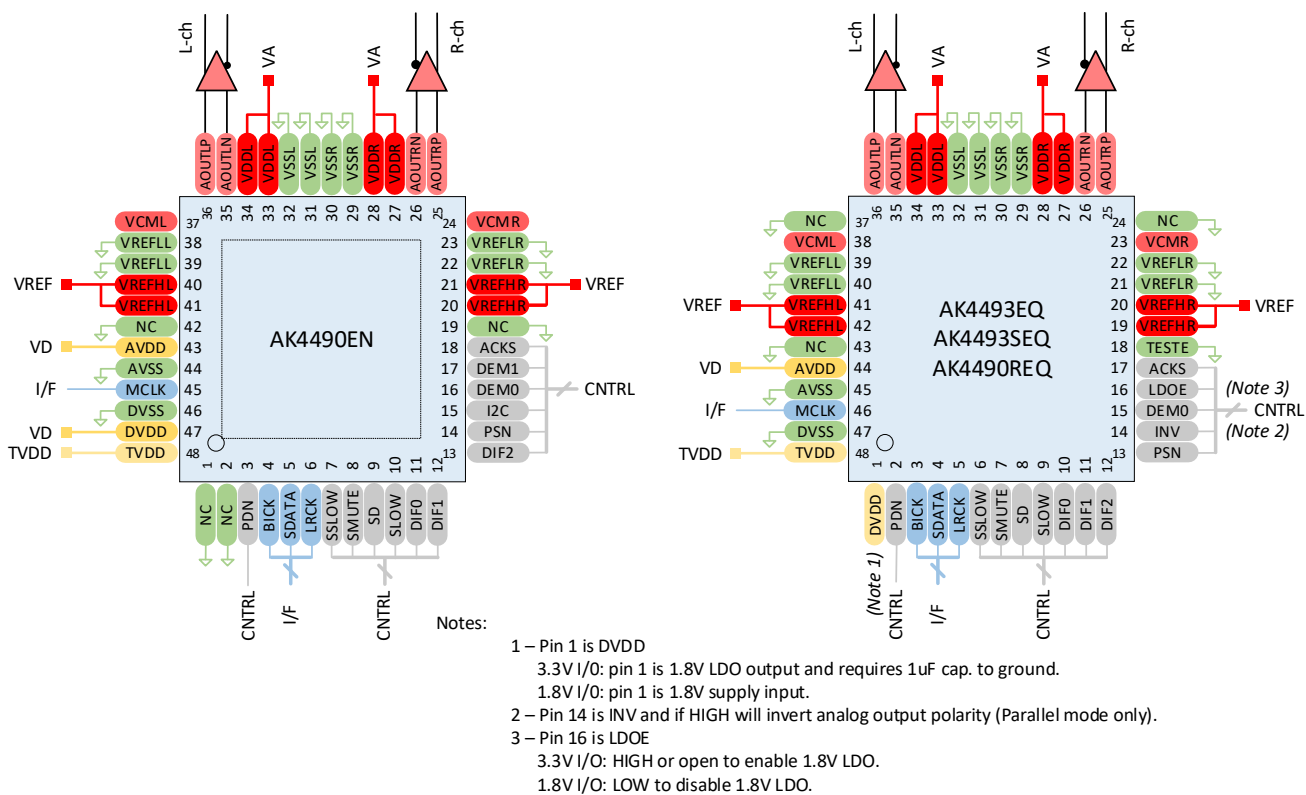


Figure 2– Pinout and circuit arrangements of the AK4490EN vs. AK4493/93S/90R

Refer to [Table 2](#) below for the summary of pin and system design changes transitioning from the AK4490EN to the AK4490R/93S (LQFP).

Table 2– Summary of changes for transitioning from AK4490EN (QFN) to AK4490R/93S (LQFP)

Pin #	Pin name (AK4490EN)	Pin name (AK4490R/93S)	Board design impact
1	NC	DVDD (1.8V)	Relocate DVDD connection from pin 47 to pin 1, noting that voltage handling is changed. For 3.3V I/O voltage connect a 1uF cap. to gnd. for the integrated 1.8V LDO output. For 1.8V I/O voltage input 1.8V supply.
2	NC	PDN	Relocate PDN conn. from pin 3 to pin 2.
3	PDN	BICK/DCLK/BCK	Relocate BICK... conn. from pin 4 to pin 3.
4	BICK/DCLK/BCK	SDATA/DSDL/DINL	Relocate SDATA... conn. from pin 5 to pin 4.
5	SDATA/DSDL/DINL	LRCK/DSDR/DINR	Relocate LRCK... conn. from pin 6 to pin 5.
6	LRCK/DSDR/DINR	SSLOW/WCK	Relocate SSLOW... conn. from pin 7 to pin 6
7	SSLOW/WCK	SMUTE/CSN	Relocate SMUTE... conn. from pin 8 to pin 7
8	SMUTE/CSN	SD/CCLK/SCL	Relocate SD... conn. from pin 9 to pin 8.
9	SD/CCLK/SCL	SLOW/CDTI/SDA	Relocate SLOW... conn. from pin 10 to pin 9
10	SLOW/CDTI/SDA	DIF0/DZFL	Relocate DIF0... conn. from pin 11 to pin 10.
11	DIF0/DZFL	DIF1/DZFR	Relocate DIF1... conn. from pin 12 to pin 11.
12	DIF1/DZFR	DIF2/CAD0	Relocate DIF2... conn. from pin 13 to pin 12.
13	DIF2/CAD0	PSN	Relocate PSN conn. from pin 14 to pin 13.
14	PSN	INV*/I2C	Relocate conn. from pin 15 I2C to pin 14 INV*/I2C. *Parallel Control mode: pin function becomes INV and if tied HIGH the DAC output polarity will be inverted.
15	I2C	DEM0*	Relocate DEM0* conn. from pin 16 to pin 15. *Parallel Control mode: tie HIGH if desired to disable De-emphasis; the AK4490EN has an internal pull-up, while the AK4490R/93S does not.
16	DEM0	LDOE	Pin changes function to LDOE. For 3.3V I/O voltage tie LDOE HIGH or leave it open to enable integrated 1.8V LDO; the AK4490EN has an internal pull-down, while the AK4490R/93S has an internal pull-up. For 1.8V I/O voltage tie LDOE LOW to disable integrated 1.8V LDO.
17	DEM1*	ACKS*/CAD1	Relocate ACKS...* conn. from pin 18 to pin 17. *Parallel Control mode: tie LOW to disable ACKS mode; the AK4490EN has an internal pull-down, while the AK4490R/93S does not.
18	ACKS/CAD1	TESTE	Pin changes function to TESTE (test mode enable with internal pull-down). Tie LOW or leave open.
19	NC	VREFHR	Relocate VREFHR conn. from pin 20 to 19.
20	VREFHR	VREFHR	(No effective change.)
21	VREFHR	VREFLR	Relocate VREFLR conn. from pin 22 to 21.
22	VREFLR	VREFLR	(No effective change.)
23	VREFLR	VCMR	Relocate conn. from pin 24 VCOMR to 23 VCMR.
24	VCOMR	NC	Pin changes to NC. Connect to ground.
25 – 36			(No change.)
37	VCOML	NC	Pin changes to NC. Connect to ground.
38	VREFLL	VCML	Relocate conn. from pin 37 VCOMR to 38 VCML.

39	VREFLL	VREFLL	(No effective change.)
40	VREFHL	VREFLL	Relocate VREFLL conn. from pin 39 to 40.
41	VREFHL	VREFHL	(No effective change.)
42	NC	VREFHL	Relocate VREFHL conn. from pin 41 to 42.
43	AVDD	NC	Relocate NC conn. (gnd) from pin 42 to 43.
44	AVSS	AVDD	Relocate AVDD conn. from pin 43 to 44.
45	MCLK	AVSS	Relocate AVSS conn. from pin 44 to 45.
46	DVSS	MCLK	Relocate MCLK conn. from pin 45 to 46.
47	DVDD	DVSS	Relocate DVSS conn. from pin 46 to 47.
48	TVDD	TVDD	For 3.3V I/O voltage, connect 3.3V supply. For 1.8V I/O voltage, connect 1.8V supply.
Thermal Pad	(included in pkg.)	(not included in pkg.)	Omit connection to analog ground plane.

Table 2 (cont.) – Summary of changes for transitioning from AK4490EN (QFN) to AK4490R/93S (LQFP)

Software compatibility

Note that while there are some register control bits added and removed to the AK4493/93S/90R to support a minor alteration of the feature set, compatibility with the AK4490 remains intact, with the exception of certain rarely used bits related to DSD full-scale signal detection and automatic muting implementation. If the application utilizes these features, consult as needed the AK4490 and AK4490R/93S datasheets.

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