

# CURRENT MIRRORS

## INTRODUCTION

### Objective

The objective of this presentation is:

- 1.) Introduce and characterize the current mirrors
- 2.) Show how to improve the performance of the current mirrors
- 3.) Demonstrate the design of current mirrors

### Outline

- Simple MOS current mirrors
- Simple BJT current mirrors
- Cascode current mirrors
- Wilson current mirrors
- Regulated-cascode current mirrors
- Summary

## SIMPLE MOS CURRENT MIRRORS

### Characterization of Current Mirrors

A current mirror is basically nothing more than a current amplifier. The ideal characteristics of a current amplifier are:

- Output current linearly related to the input current,  $i_{out} = A_i i_{in}$
- Input resistance is zero
- Output resistance is infinity

In addition, we have the characteristic  $V_{MIN}$  which applies not only to the output but also the input.

- $V_{MIN}(in)$  is the range of input voltage over which the input resistance is not small
- $V_{MIN}(out)$  is the range of the output voltage over which the output resistance is not large

Graphically:

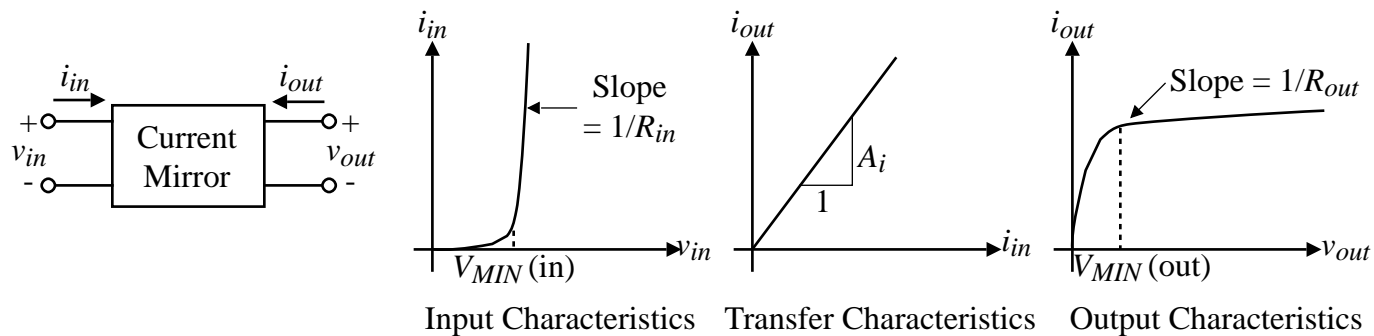


Fig. 4.4-1

Therefore, we will focus on  $R_{out}$ ,  $R_{in}$ ,  $V_{MIN}(out)$ ,  $V_{MIN}(in)$ , and  $A_i$  to characterize the current mirror.

### Simple MOS Current Mirror

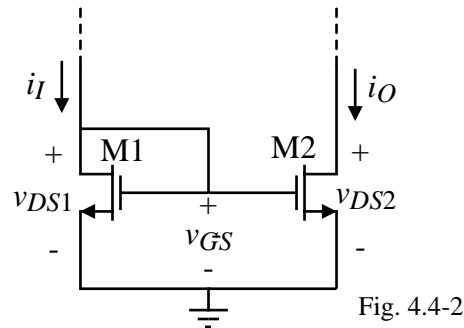


Fig. 4.4-2

Assume that  $v_{DS2} > v_{GS} - V_{T2}$ , then

$$\frac{i_O}{i_I} = \left( \frac{L_1 W_2}{W_1 L_2} \right) \left( \frac{V_{GS} - V_{T2}}{V_{GS} - V_{T1}} \right)^2 \left[ \frac{1 + \lambda v_{DS2} \left( \frac{K_2'}{K_1'} \right)}{1 + \lambda v_{DS1} \left( \frac{K_2'}{K_1'} \right)} \right]$$

If the transistors are matched, then  $K_1' = K_2'$  and  $V_{T1} = V_{T2}$  to give,

$$\frac{i_O}{i_I} = \left( \frac{L_1 W_2}{W_1 L_2} \right) \left( \frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}} \right)$$

If  $v_{DS1} = v_{DS2}$ , then

$$\frac{i_O}{i_I} = \left( \frac{L_1 W_2}{W_1 L_2} \right)$$

Therefore the sources of error are 1.)  $v_{DS1} \neq v_{DS2}$  and 2.) M1 and M2 are not matched.

### Influence of the Channel Modulation Parameter, $\lambda$

If the transistors are matched and the W/L ratios are equal, then

$$\frac{i_O}{i_I} = \frac{1 + \lambda v_{DS2}}{1 + \lambda v_{DS1}}$$

assuming that the channel modulation parameter is the same for both transistors ( $L_1 = L_2$ ).

Ratio error (%) versus drain voltage difference:

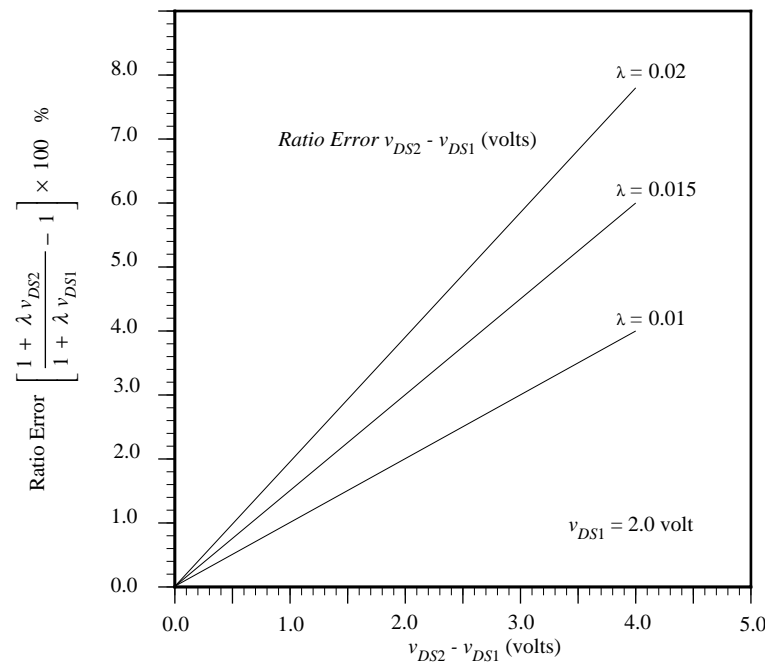


Fig. 4.4-3

Note that one could use this effect to measure  $\lambda$ .

Measure  $V_{DS1}$ ,  $V_{DS2}$ ,  $i_I$  and  $i_O$  and solve the above equation for the channel modulation parameter,  $\lambda$ .

### Influence of Mismatched Transistors

Assume that  $v_{DS1} = v_{DS2}$  and that  $K_1' \neq K_2'$  and  $V_{T1} \neq V_{T2}$ . Therefore we have

$$\frac{i_O}{i_I} = \frac{K_2'(v_{GS} - V_{T2})^2}{K_1'(v_{GS} - V_{T1})^2}$$

How do you analyze the mismatch? Use plus and minus worst case approach. Define

$$\begin{aligned} \Delta K' &= K_2' - K_1' & K' &= 0.5(K_2' + K_1') & \Delta V_T &= V_{T2} - V_{T1} & \text{and } V_T &= 0.5(V_{T1} + V_{T2}). \\ \therefore K_1' &= K' - 0.5\Delta K' & K_2' &= K' + 0.5\Delta K' & V_{T1} &= V_T - 0.5\Delta V_T & \text{and } V_{T2} &= V_T + 0.5\Delta V_T \end{aligned}$$

Substituting these terms into the above equation gives,

$$\frac{i_O}{i_I} = \frac{(K' + 0.5\Delta K')(v_{GS} - V_T - 0.5\Delta V_T)^2}{(K' - 0.5\Delta K')(v_{GS} - V_T + 0.5\Delta V_T)^2} = \frac{\left(1 + \frac{\Delta K'}{2K'}\right) \left(1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2}{\left(1 - \frac{\Delta K'}{2K'}\right) \left(1 + \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2}$$

Assuming that the terms added to or subtracted from "1" are smaller than unity gives

$$\frac{i_O}{i_I} \approx \left(1 + \frac{\Delta K'}{2K'}\right) \left(1 + \frac{\Delta K'}{2K'}\right) \left(1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2 \left(1 - \frac{\Delta V_T}{2(v_{GS} - V_T)}\right)^2 \quad \text{Uses the approximation } 1/(1 \pm \epsilon) \approx 1 \mp \epsilon$$

Retaining only first order products gives

$$\frac{i_O}{i_I} \approx 1 + \frac{\Delta K'}{K'} - \frac{2\Delta V_T}{(v_{GS} - V_T)}$$

Assume  $\Delta K'/K' = \pm 5\%$  and  $\Delta V_T/(v_{GS} - V_T) = \pm 10\%$ .

$$\therefore i_O/i_I \approx 1 \pm 0.05 \pm (-0.20) = 1 \pm (0.25) \quad \Rightarrow \quad \pm 15\% \text{ error in gain if tolerances are correlated.}$$

### Illustration of the Offset Voltage Error Influence

Assume that  $V_{T1} = 0.7\text{V}$  and  $K'W/L = 110\mu\text{A/V}^2$ .

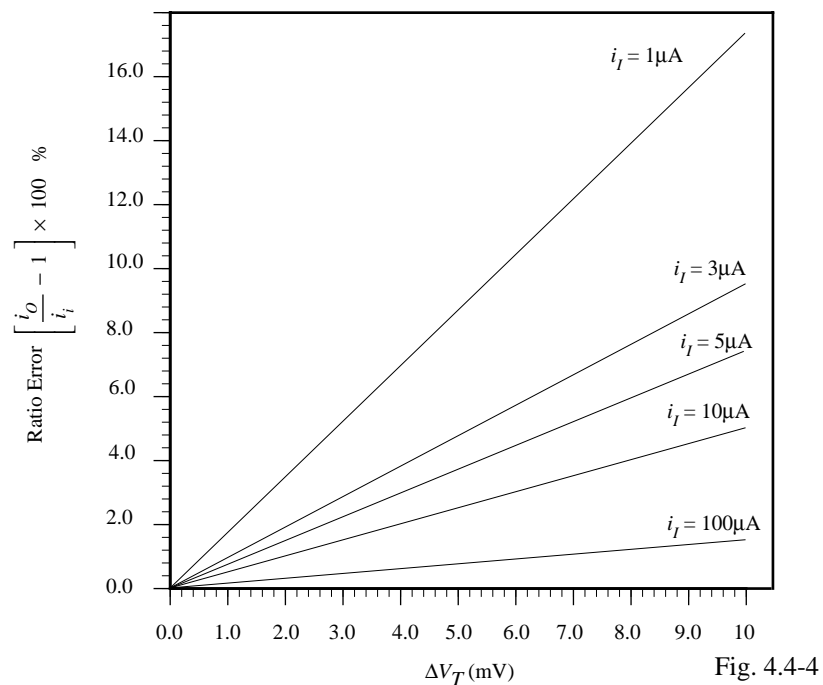


Fig. 4.4-4

Key: Make the part of  $V_{GS}$  that causes the current to flow,  $V_{ON}$ , more significant than  $V_T$ .

### Influence of Error in Aspect Ratio of the Transistors

#### Example 1 - Aspect Ratio Errors in Current Mirrors

Figure 4.4-4 shows the layout of a one-to-four current amplifier. Assume that the lengths are identical ( $L_1 = L_2$ ) and find the ratio error if  $W_1 = 5 \pm 0.1 \mu\text{m}$ . The actual widths of the two transistors are

$$W_1 = 5 \pm 0.1 \mu\text{m} \text{ and } W_2 = 20 \pm 0.1 \mu\text{m}$$

#### Solution

We note that the tolerance is not multiplied by the nominal gain factor of 4. The ratio of  $W_2$  to  $W_1$  and consequently the gain of the current amplifier is

$$\frac{i_O}{i_I} = \frac{W_2}{W_1} = \frac{20 \pm 0.1}{5 \pm 0.1} = 4 \left( \frac{1 \pm \frac{0.1}{20}}{1 \pm \frac{0.1}{5}} \right) \approx 4 \left( 1 \pm \frac{0.1}{20} \right) \left( 1 - \frac{\pm 0.1}{5} \right) \approx 4 \left( 1 \pm \frac{0.1}{20} - \frac{\pm 0.4}{20} \right) = 4 - (\pm 0.06)$$

where we have assumed that the variations would both have the same sign (correlated). It is seen that this ratio error is 1.5% of the desired current ratio or gain.

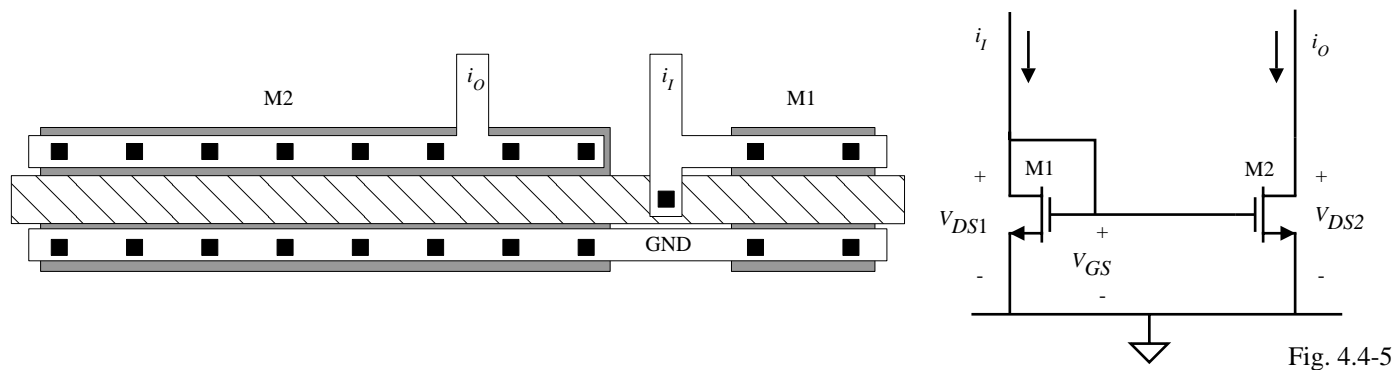


Fig. 4.4-5

### Influence of Error in Aspect Ratio of the Transistors-Continued

#### Example 2 - Reduction of the Aspect Ratio Errors in Current Mirrors

Use the layout technique illustrated in Fig. 4.4-5 and calculate the ratio error of a current amplifier having the specifications of the previous example.

#### Solutions

The actual widths of M1 and M2 are

$$W_1 = 5 \pm 0.1 \mu\text{m} \text{ and } W_2 = 4(5 \pm 0.1) \mu\text{m}$$

The ratio of  $W_2$  to  $W_1$  and consequently the current gain is given below and is for all practical purposes independent of layout error.

$$\frac{i_O}{i_I} = \frac{4(5 \pm 0.1)}{5 \pm 0.1} = 4$$

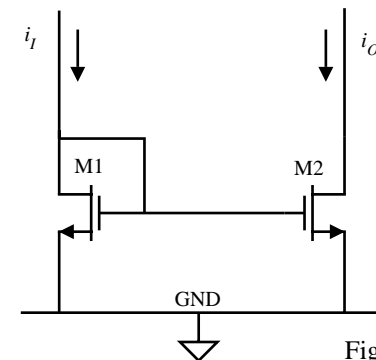
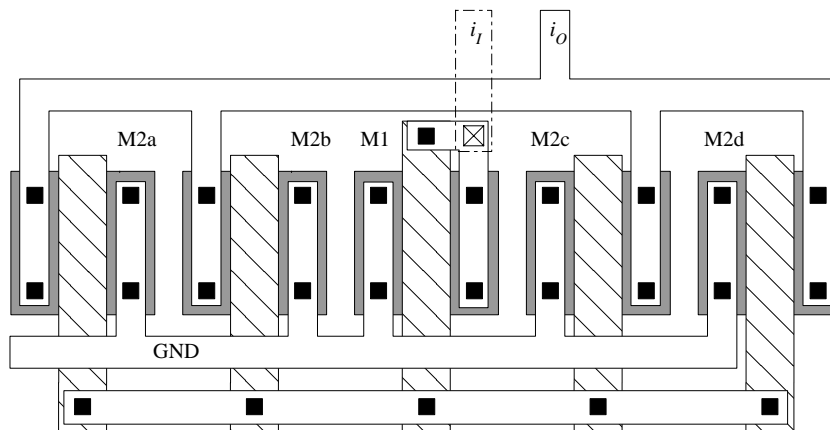


Fig. 4.4-6

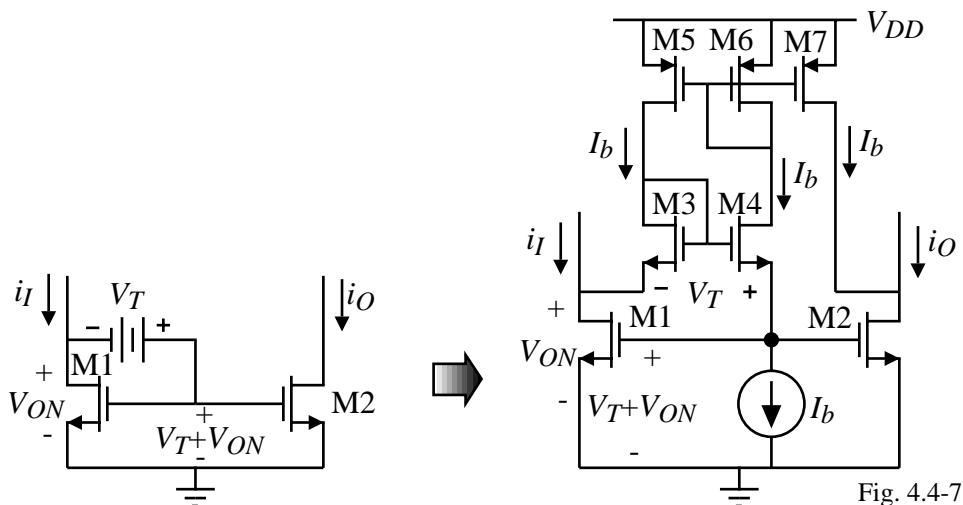


### Summary of the Simple MOS Current Mirror/Amplifier

- Minimum input voltage is  $V_{MIN}(in) = V_T + V_{ON}$

Okay, but could be reduced to  $V_{ON}$ .

Principle:

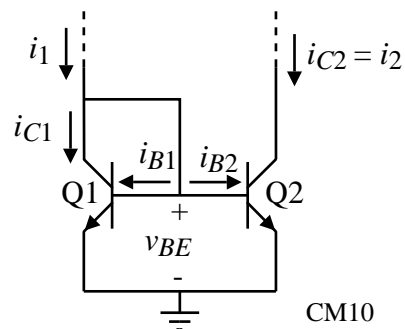


Will deal with later in low voltage op amps.

- Minimum output voltage is  $V_{MIN}(out) = V_{ON}$
- Output resistance is  $R_{out} = \frac{1}{\lambda_D}$
- Input resistance is  $R_{in} \approx \frac{1}{g_m}$
- Current gain accuracy is poor because  $v_{DS1} \neq v_{DS2}$

## SIMPLE BJT CURRENT MIRRORS

### Characterization of a Simple BJT Current Mirror



$$R_{out} = r_{o2} = \frac{V_{A2}}{I_{C2}}$$

$$R_{in} \approx \frac{1}{g_{m1}} = \frac{V_t}{I_{C1}}$$

$$V_{MIN}(\text{out}) = v_{CE}(\text{sat}) \approx 0.2\text{V}$$

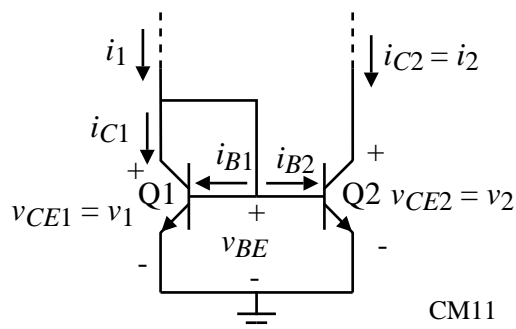
$$V_{MIN}(\text{in}) = V_{BE} \approx 0.6 \text{ to } 0.7\text{V}$$

and

$$A_i = \frac{I_{s2}}{I_{s1}} \quad \text{if the transistors are matched and } \beta = \infty.$$

### Simple BJT Current Mirror Matching

Circuit:



$$i_1 = i_{C1} + i_{B1} + i_{B2} = i_{E1} + i_{B2} = \frac{i_{C1}}{\alpha_{F1}} + i_{B2}$$

$$i_{C1} = \left(1 + \frac{v_{CE1}}{V_{A1}}\right) I_{s1} \exp(v_{BE}/V_t)$$

and

$$i_{C2} = i_2 = \left(1 + \frac{v_{CE2}}{V_{A2}}\right) I_{s2} \exp(v_{BE}/V_t)$$

Now,

$$i_1 = \left(1 + \frac{v_{CE1}}{V_{A1}}\right) \left(\frac{I_{s1}}{\alpha_{F1}}\right) \exp(v_{BE}/V_t) + i_{B2} \quad \text{and} \quad i_{B2} = \frac{i_{C2}}{\beta_{F2}} = \frac{i_2}{\beta_{F2}} = \left[\frac{1 - \alpha_{F2}}{\alpha_{F2}}\right] \left[1 + \frac{v_2}{V_{A2}}\right] I_{s2} \exp(v_{BE}/V_t)$$

$$\therefore i_1 = \left\{ \left(1 + \frac{v_1}{V_{A1}}\right) \left(\frac{I_{s1}}{\alpha_{F1}}\right) + \left[\frac{1 - \alpha_{F2}}{\alpha_{F2}}\right] \left[1 + \frac{v_2}{V_{A2}}\right] I_{s2} \right\} \exp(v_{BE}/V_t)$$

Finally,

$$\frac{i_2}{i_1} = \frac{\left(1 + \frac{v_2}{V_{A2}}\right)}{\left(1 + \frac{v_1}{V_{A1}}\right) \left(\frac{I_{s1}}{\alpha_{F1}}\right) + \left[\frac{1 - \alpha_{F2}}{\alpha_{F2}}\right] \left[1 + \frac{v_2}{V_{A2}}\right] I_{s2}}$$

### Simple BJT Current Mirror Matching - Continued

Using a Taylor series expansion and ignoring the second-order terms, we have

$$\frac{i_2}{i_1} \approx \frac{I_{S2}}{\left(1 + \frac{v_1}{V_{A1}} - \frac{v_2}{V_{A2}}\right) \left(\frac{I_{S1}}{\alpha_{F1}}\right) + \left[\frac{(1 - \alpha_{F2})}{\alpha_{F2}}\right] I_{S2}}$$

For large  $\beta_F$  ( $\alpha_F \approx 1$ ):

$$\frac{i_2}{i_1} \approx \frac{I_{S2}}{\left(1 + \frac{v_1}{V_{A1}} - \frac{v_2}{V_{A2}}\right) I_{S1}}$$

Again using Taylor-series expansion:

$$\frac{i_2}{i_1} \approx \left(\frac{I_{S2}}{I_{S1}}\right) \left(1 - \frac{v_1}{V_{A1}} + \frac{v_2}{V_{A2}}\right)$$

Let  $\Delta I_S = I_{S2} - I_{S1}$  and  $I_S \approx I_{S1} \approx I_{S2}$

$$\frac{i_2}{i_1} \approx \left(1 + \frac{\Delta I_S}{I_S}\right) \left(1 - \frac{v_1}{V_{A1}} + \frac{v_2}{V_{A2}}\right)$$

For  $v_1 = V_{BE} = 0.7\text{V}$ ,  $v_2 = 5\text{V}$ ,  $\frac{\Delta I_S}{I_S} = 0.02$ ,  $V_A = 50$

$$\frac{i_2}{i_1} \approx 1.11 > 11\% \text{ error due primarily to mismatch in } R_{out} \text{ (} v_1 \text{ and } v_2 \text{)}$$

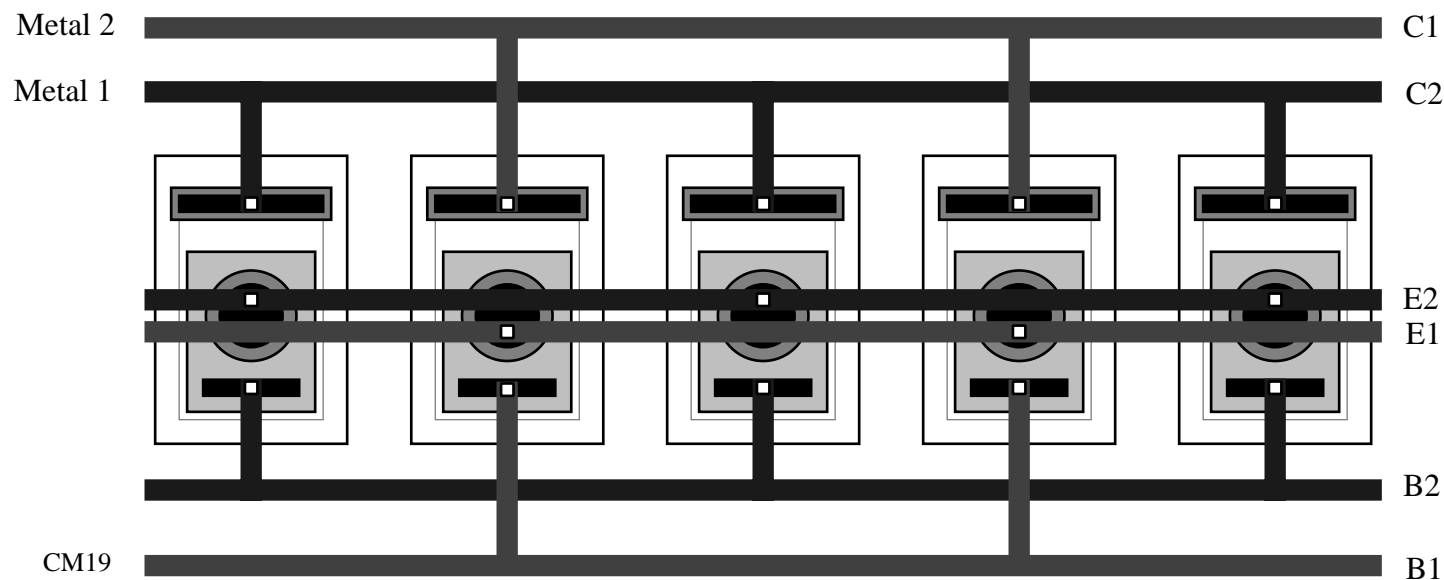
### Geometrical Influence on BJT Matching

If everything is ideal ( $\beta_F = \infty$  and  $V_{CE1} = V_{CE2}$ ), the matching of the currents is determined by the matching of the saturation currents,  $I_s$ , which is given as

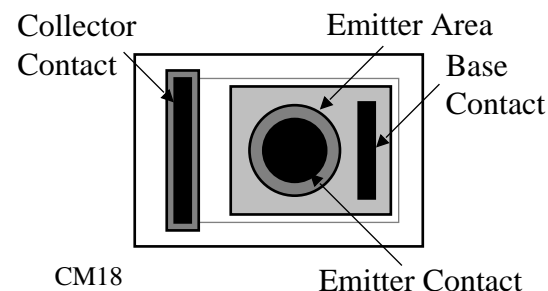
$$I_s = \frac{qn_i^2 D_n}{N_A W_B (V_{CB})} A_E = \frac{qn_i^2 D_n}{Q_B (V_{CB})} A_E$$

Therefore, the transistor matching directly depends on how well the emitter areas are matched.

If a current gain greater than 1 is required, the emitter areas should be implemented as follows:



Current gain of the above structure is 1.5.



**Rules for Matching of NPN BJT Transistors<sup>†</sup>**

1. Use identical emitter geometries.
2. The emitter diameter should equal 2-10 times the minimum allowed diameter.
3. Maximize the emitter area-to-periphery ratio (circle the best, square okay).
4. Place matched transistors in close proximity
5. Keep the layout of matched transistors as compact as possible.
6. Construct ratioed pairs and quads using even integer ratios between 4:1 and 16:1
7. Place matched transistors far away from power devices.
8. Place matched transistor in low-stress areas (thermal and physical).
9. Place moderately or precisely matched transistors on axes of symmetry of the die.
10. Do not allow the buried layer shadow to intersect matched emitters (must overlay the emitter area).
11. Place emitters far enough apart to avoid interactions.
12. Increase the base overlap of moderately or precisely matched emitters.
13. Operate matched transistors on the flat portion of the beta curve.
14. The contact geometry should match the emitter geometry (circular contact for circular structure, square contact for square structure, etc.).
15. Consider using emitter degeneration.

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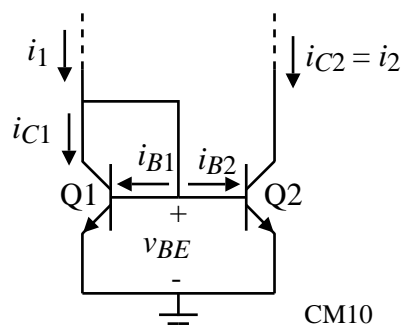
<sup>†</sup> Alan Hastings, "The Art of Analog Layout", Chapter 9, 1998 (Unpublished text, VRG1@msg.ti.com)

**Rules for Matching Lateral PNP Transistors**

1. Use identical emitter and collector geometries.
2. Use minimum-size emitters for matched transistors.
3. Field plate the base region of matched lateral PNP transistors.
4. Split-collector lateral PNP transistors can achieve moderate matching.
5. Place matched transistors in close proximity.
6. If possible, avoid constructing VPTAT circuits from ratioed lateral PNP transistors.
7. Place matched transistors far away from power devices.
8. Place matched transistor in low-stress areas (thermal and physical).
9. Place moderately or precisely matched transistors on axes of symmetry of the die.
10. Do not allow the buried layer shadow to intersect matched emitters (must overlay the emitter area).
11. Operate matched lateral PNP transistors near peak beta.
12. The contact geometry should match the emitter geometry (circular contact for circular structure, square contact for square structure, etc.).
13. Consider using emitter degeneration.

### Simple BJT Current Mirror for Finite $\beta$

Circuit:



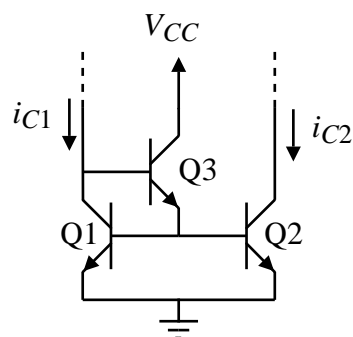
If the transistors are matched and  $v_{CE1} = v_{CE2}$ , then  $i_{C1} = i_{C2}$  but

$$i_{C1} = i_1 - 2i_B = i_1 \left( 1 + \frac{2}{\beta} \right)$$

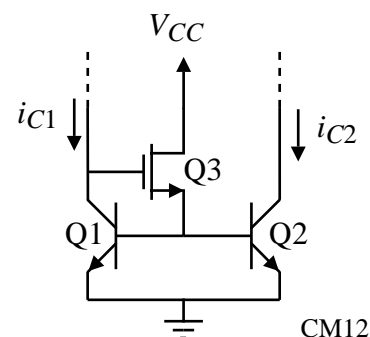
$$\therefore A_i = \frac{i_2}{i_1} = \frac{1}{1 + \frac{2}{\beta}}$$

If  $\beta_F$  is small then appreciable error is introduced into the current gain.

Solutions to this problem:



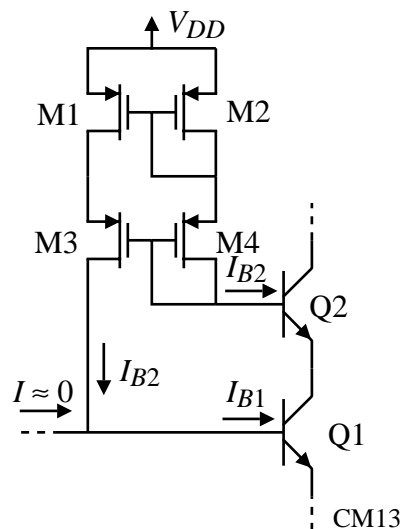
or





### Base-Current Cancellation

In a BiCMOS process, base current cancellation is possible and using the following technique.



If Q1 and Q2 are matched, then  $I_{C1} \approx I_{C2}$  and  $I_{B1} \approx I_{B2}$ .

The cascode current mirror is used to make sure that  $I_{B1} = I_{B2}$ .

## CASCODE CURRENT MIRRORS

### MOS Cascode Current Mirror

Improving the output resistance:

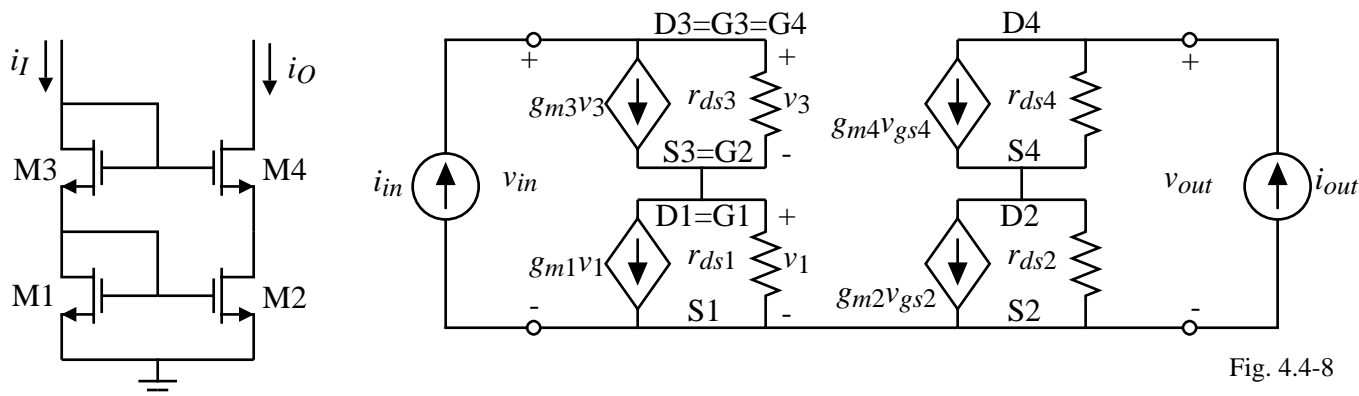


Fig. 4.4-8

- $R_{out}$ :

$$v_{out} = r_{ds4}(i_{out} - g_{m4}v_{gs4}) + r_{ds2}(i_{out} - g_{m2}v_{gs2})$$

$$\text{But, } i_{in} = 0 \text{ so that } v_1 = v_3 = 0 \Rightarrow v_{gs4} = -v_{s4} = -i_{out}r_{ds2} \text{ and } v_{gs2} = 0$$

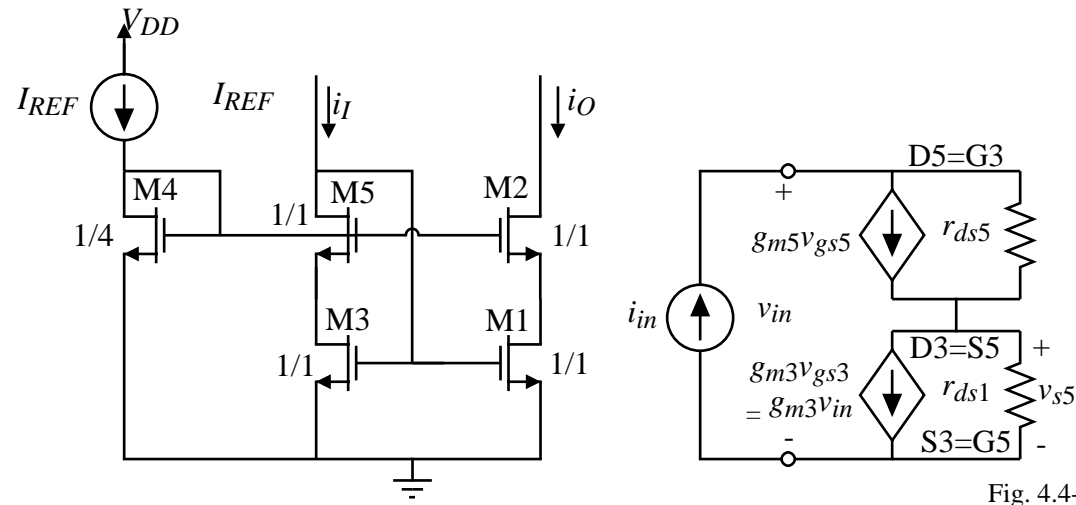
$$\therefore v_{out} = i_{out}[r_{ds4} + r_{ds2} + g_{m4}r_{ds2}r_{ds4}] \approx r_{ds2}g_{m4}r_{ds4}$$

- $R_{in}$ :

$$R_{in} = \frac{1}{g_{m3}} \parallel r_{ds3} + \frac{1}{g_{m1}} \parallel r_{ds1} \approx \frac{1}{g_{m1}} + \frac{1}{g_{m3}} \approx \frac{2}{g_m}$$

- $V_{MIN}(\text{out}) = V_T + 2V_{ON}$
- $V_{MIN}(\text{in}) = 2(V_T + V_{ON})$
- Current gain match: Excellent since  $v_{DS1} = v_{DS2}$

### Large Output Swing Cascode Current Mirror



- $R_{out} \approx g_{m2}r_{ds2}r_{ds1}$
- $R_{in} = ?$   $v_{in} = r_{ds5}(i_{in} - g_{m5}v_{gs5}) + v_{s5} = r_{ds5}(i_{in} + g_{m5}v_{s5}) + v_{s5} = r_{ds5}i_{in} + (1 + g_{m5}r_{ds5})v_{s5}$

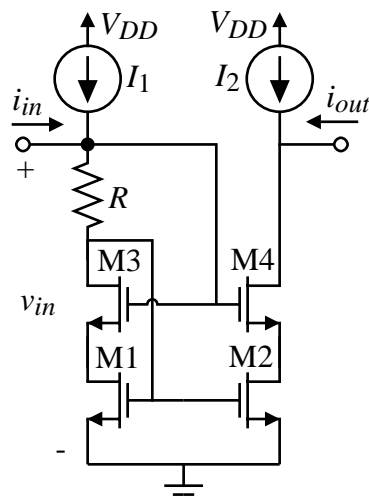
But,  $v_{s5} = r_{ds3}(i_{in} - g_{m3}v_{in})$

$$\therefore v_{in} = r_{ds5}i_{in} + (1 + g_{m5}r_{ds5})r_{ds3}i_{in} - g_{m3}r_{ds3}(1 + g_{m5}r_{ds5})v_{in}$$

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{r_{ds5} + r_{ds3} + r_{ds3}g_{m5}r_{ds5}}{g_{m3}r_{ds3}(1 + g_{m5}r_{ds5})} \blacktriangleright \frac{1}{g_{m3}}$$

- $V_{MIN}(\text{out}) = 2V_{ON}$
- $V_{MIN}(\text{in}) = V_T + V_{ON}$
- Current gain is excellent because  $v_{DS1} = v_{DS3}$ .

### Self-Biased Cascode Current Mirror



Self-biased, cascode current mirror

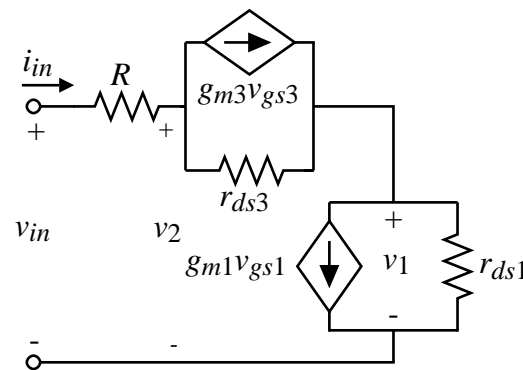
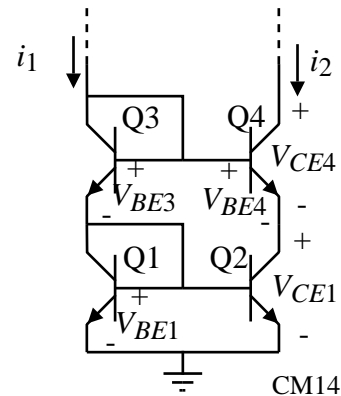
Small-signal model to calculate  $R_{in}$ .

Fig. 4.4-10

- $R_{in} = ?$   $v_{in} = i_{in}R + r_{ds3}(i_{in} - g_{m3}v_{gs3}) + r_{ds1}(i_{in} - g_{m1}v_{gs1})$   
 But,  $v_{gs1} = v_{in} - i_{in}R$  and  $v_{gs3} = v_{in} - r_{ds1}(i_{in} - g_{m1}v_{gs1}) = v_{in} - r_{ds1}i_{in} + g_{m1}r_{ds1}(v_{in} - i_{in}R)$   
 $\therefore v_{in} = i_{in}R + r_{ds3}i_{in} - g_{m3}r_{ds3}[v_{in} - r_{ds1}i_{in} + g_{m1}r_{ds1}(v_{in} - i_{in}R)] + r_{ds1}[i_{in} - g_{m1}(v_{in} - i_{in}R)]$   
 $v_{in}[1 + g_{m3}r_{ds3} + g_{m1}r_{ds1}g_{m3}r_{ds3} + g_{m1}r_{ds1}] = i_{in}[R + r_{ds1} + r_{ds3} + g_{m3}r_{ds3}r_{ds1} + g_{m1}r_{ds1}g_{m3}r_{ds3}R]$   

$$R_{in} = \frac{R + r_{ds1} + r_{ds3} + g_{m3}r_{ds3}r_{ds1} + g_{m1}r_{ds1}g_{m3}r_{ds3}R}{1 + g_{m3}r_{ds3} + g_{m1}r_{ds1}g_{m3}r_{ds3} + g_{m1}r_{ds1}} \uparrow \frac{1}{g_{m1}} + R$$
- $R_{out} \approx g_{m4}r_{ds4}r_{ds2}$
- $V_{MIN}(in) = V_T + 2V_{ON}$
- $V_{MIN}(out) = 2V_{ON}$
- Current gain matching is excellent

### BJT Cascode Current Mirror



#### Advantages:

Because  $V_{CE1} = V_{CE2}$ , this mirror will have very good matching if  $\beta_F$  is very large.

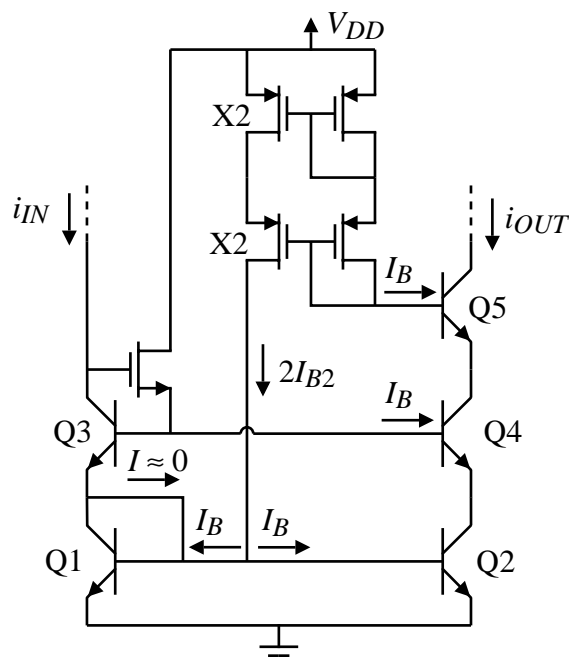
Output resistance large because of cascoded output ( $R_{out} \approx \beta_{F4} r_{o2}$ )

#### Disadvantages:

$$V_{MIN}(\text{out}) = V_{BE1} + v_{CE4}(\text{sat})$$

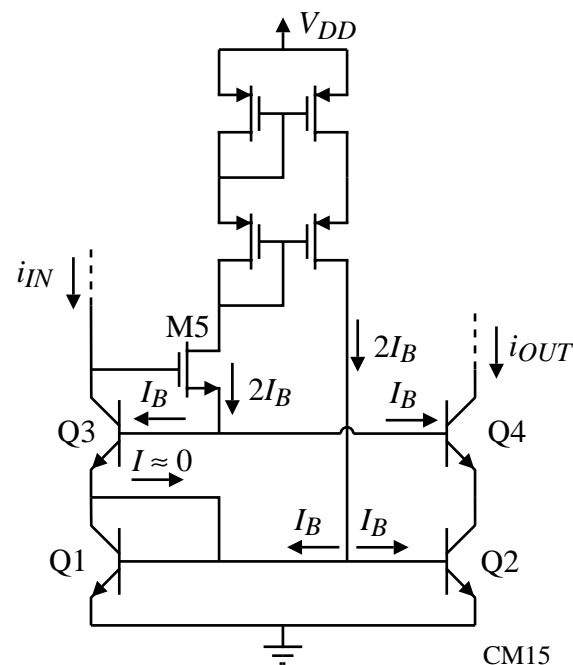
$$V_{MIN}(\text{in}) = V_{BE1} + V_{BE3} = 2V_{BE}$$

### Improving the Matching of the BJT Cascode Current Mirror



Achieves the desired base current cancellation

However, there are three transistors stacked at the output which will cause a large  $V_{MIN}$

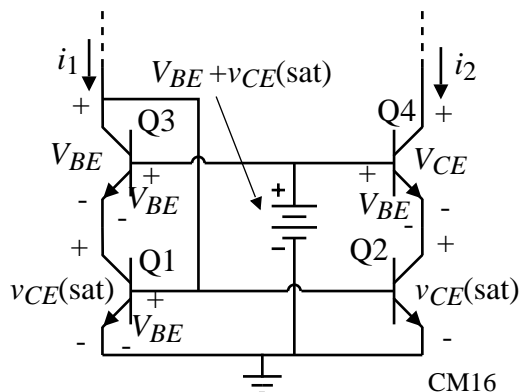


Achieves the desired base current cancellation using only two stacked transistors

$$V_{MIN} = V_{BE} + v_{CE}(\text{sat})$$

### Improving $V_{MIN}$ of the BJT Cascode Current Mirror

Use the “trick” of freeing the voltage at the bases of the cascode transistors to get,



Advantages:

$$V_{MIN(out)} = 2v_{CE(sat)}$$

$$R_{out} \approx \beta_F r_o$$

$$V_{MIN(in)} = V_{BE} \text{ (lowest possible without using extreme methods)}$$

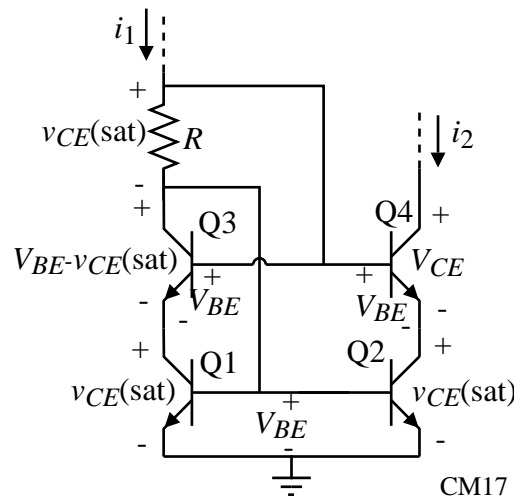
Disadvantages:

Screwed up the current mismatch. Okay if  $\beta_F$  is large or you can use another transistor but  $V_{MIN(in)}$  will increase.

Requires a battery of  $V_{BE} + v_{CE(sat)}$

### Self-Biased, $V_{MIN}(\text{out})$ BJT Cascode Current Mirror

Can eliminate the battery using the self-biased concept as illustrated below.



Design  $R$  so that  $R = \frac{v_{CE}(\text{sat})}{I_1}$

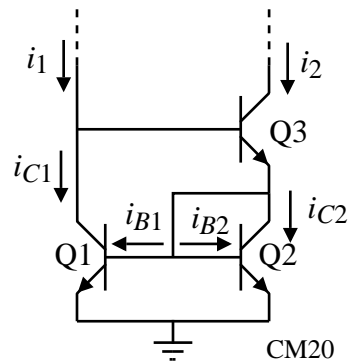
Comments:

- Minimum  $V_{MIN}(\text{out})$  can be obtained ( $2v_{CE}(\text{sat})$ )
- The  $V_{MIN}(\text{in})$  is equal to  $V_{BE} + v_{CE}(\text{sat})$
- Still have current mismatch if  $\beta_F$  is not large (can use two more transistors to eliminate the mismatch)



## WILSON CURRENT MIRROR

### BJT Wilson Current Mirror



$$i_2 + i_{B3} = i_{C2} + i_{B1} + i_{B2} \rightarrow i_2 \left(1 + \frac{1}{\beta_F}\right) = i_{C2} \left(1 + \frac{1}{\beta_F}\right) + \frac{i_{C1}}{\beta_F}$$

$$\therefore i_2 = i_{C2} \left(1 + \frac{1}{\beta_F}\right) = i_{C2} \left(\frac{2 + \beta_F}{1 + \beta_F}\right)$$

$$\text{Solving for } i_{C2} \text{ gives } i_{C2} = \left(\frac{1 + \beta_F}{2 + \beta_F}\right) i_2$$

Substituting for  $i_{C1} = i_{C2}$  into  $i_1 = i_{C1} + i_{B3} = i_{C1} + \frac{i_2}{\beta_F}$  gives

$$i_1 = \left(\frac{1 + \beta_F}{2 + \beta_F}\right) i_2 + \frac{i_2}{\beta_F} = i_2 \left(\frac{1 + \beta_F}{2 + \beta_F} + \frac{1}{\beta_F}\right) = i_2 \left(\frac{\beta_F^2 + 2\beta_F + 1}{\beta_F(\beta_F + 2)}\right) \Rightarrow \frac{i_2}{i_1} = \frac{\beta_F(\beta_F + 2)}{\beta_F^2 + 2\beta_F + 1}$$

How does the Wilson current source work?

Negative feedback -

If  $i_2$  increases (because  $v_{OUT}$  increases), then the voltage at the base of Q1 increases.

The increase of voltage at the base of Q1 appears as a decrease at the base of Q3.

Therefore, the original increase in  $i_2$  is opposed.

It can be shown that  $R_{out} \approx 0.5\beta_F r_o$ , however,  $V_{MIN}(out) = V_{BE} + v_{CE}(sat)$  and  $V_{MIN}(in) = 2V_{BE}$

Wilson current mirror suffers from poor matching ( $v_{CE1} = 2v_{CE2}$ )

### Wilson MOS Current Mirror

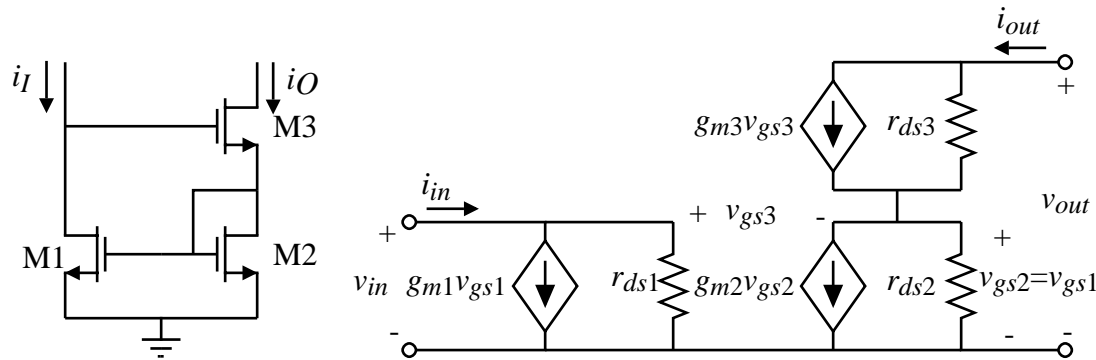


Fig. 4.4-11

Uses negative series feedback to achieve higher output resistance.

- $R_{out} = ? (i_{in}=0)$        $v_{out} = r_{ds2}(i_{out} - g_{m3}v_{gs3}) + v_{gs2}$

$$v_{gs2} = \frac{i_{out}}{g_{m2} + g_{ds2}} = \frac{r_{ds2}i_{out}}{1 + g_{m2}r_{ds2}} \quad \text{and} \quad v_{gs3} = -g_{m1}r_{ds1}v_{gs2} - v_{gs2} = -(1 + g_{m1}r_{ds1})v_{gs2}$$

$$\therefore v_{out} = r_{ds2}i_{out} + g_{m3}r_{ds2}(1 + g_{m1}r_{ds1})v_{gs2} = i_{out} \left[ r_{ds3} + r_{ds2} \left( \frac{1 + g_{m3}r_{ds2} + g_{m1}r_{ds1}g_{m3}r_{ds3}}{1 + g_{m2}r_{ds2}} \right) \right]$$

$$R_{out} = r_{ds3} + r_{ds2} \left( \frac{1 + g_{m3}r_{ds2} + g_{m1}r_{ds1}g_{m3}r_{ds3}}{1 + g_{m2}r_{ds2}} \right) \approx \frac{g_{m1}r_{ds1}g_{m3}r_{ds3}}{g_{m2}}$$

**Wilson Current Mirror - Continued**

- $R_{in} = ?$  ( $v_{out} = 0$ )

$$i_{in} \approx g_{m1}v_{gs1} = \frac{g_{m1}g_{m3}v_{gs3}}{g_{m2}+g_{ds2}+g_{ds3}} \approx \frac{g_{m1}g_{m3}v_{gs3}}{g_{m2}}$$

$$v_{gs3} = v_{in} - v_{gs1} = v_{in} - \frac{g_{m1}g_{m3}v_{gs3}}{g_{m2}} \Rightarrow v_{gs3} = \frac{v_{in}}{1 + \frac{g_{m1}g_{m3}}{g_{m2}}}$$

$$\therefore i_{in} \approx \frac{g_{m1}g_{m3}v_{in}}{g_{m2}+g_{m3}} \Rightarrow R_{in} = \frac{g_{m2}+g_{m3}}{g_{m1}g_{m3}}$$

- $V_{MIN}(in) = 2(V_T + V_{ON})$
- $V_{MIN}(out) = V_T + 2V_{ON}$
- Current gain matching - poor,  $v_{DS1} \neq v_{DS2}$

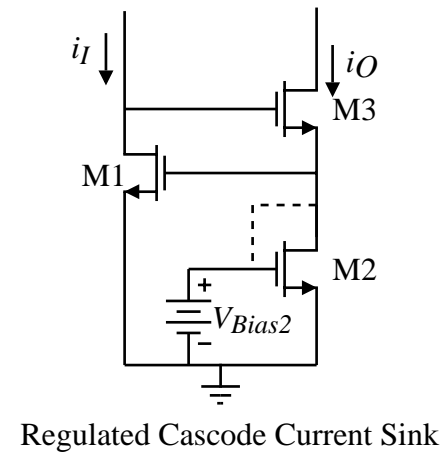
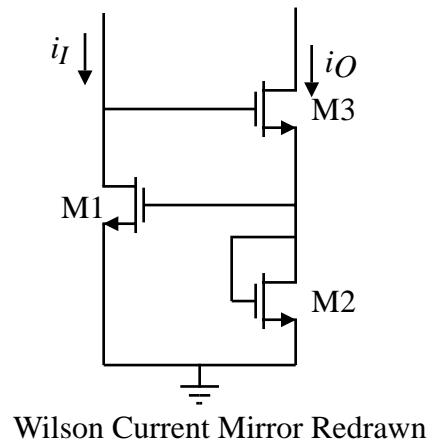
**Evolution of the Regulated Cascode Current Mirror from the Wilson Current Mirror**

Fig. 4.4-12

## REGULATED CASCODE CURRENT MIRROR

### MOS Regulated Cascode Current Mirror

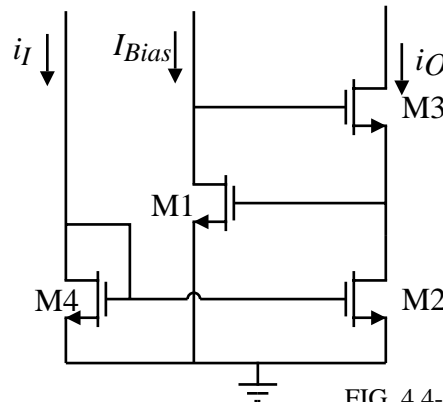
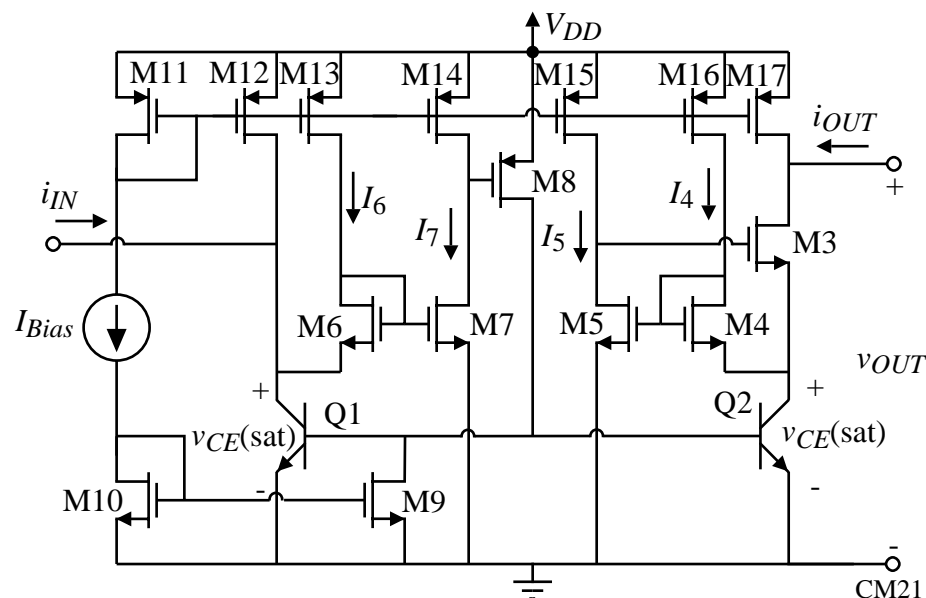


FIG. 4.4-13

- $R_{out} \approx g_m^2 r_{ds}^3$
- $R_{in} \approx \frac{1}{g_{m4}}$
- $V_{MIN}(out) = V_T + 2V_{ON}$  (Can be reduced to  $2V_{ON}$ )
- $V_{MIN}(in) = V_T + V_{ON}$  (Can be reduced to  $V_{ON}$ )
- Current gain matching - good as long as  $v_{DS4} = v_{DS2}$

## BiCMOS Regulated Cascode Current Mirror

Circuit:



Constraints:

Let  $I_4 = I_6$  and  $I_5 = I_6$ . If the  $W/L$  values of M4-M7 are equal than these currents can be used to set the collector-emitter voltages of Q1 and Q2.

$$R_{in} \approx \frac{(g_{ds7} + g_{ds14})(g_{\pi1} + g_{\pi2})}{g_{m1}g_{m7}g_{m8}}, \quad R_{out} \approx r_{o1}g_{m3}r_{ds3}g_{m5}(r_{ds5} \parallel r_{ds8}), \quad V_{MIN}(\text{out}) = V_{MIN}(\text{in}) = v_{CE}(\text{sat})$$

and the current matching will be excellent.

## SUMMARY

Summary of MOS Current Mirrors

Current Mirror	Accuracy	Output Resistance	Input Resistance	Minimum Output Voltage	Minimum Input Voltage
Simple	Poor	$r_{ds}$	$\frac{1}{g_m}$	$V_{ON}$	$V_T + V_{ON}$
Cascode	Excellent	$g_m r_{ds}^2$	$\frac{2}{g_m}$	$V_T + 2V_{ON}$	$2(V_T + V_{ON})$
Wide Output Swing Cascode	Excellent	$g_m r_{ds}^2$	$\frac{1}{g_m}$	$2V_{ON}$	$V_T + V_{ON}$
Self-biased Cascode	Excellent	$g_m r_{ds}^2$	$R + \frac{1}{g_m}$	$2V_{ON}$	$V_T + 2V_{ON}$
Wilson	Poor	$g_m r_{ds}^2$	$\frac{2}{g_m}$	$2(V_T + V_{ON})$	$V_T + 2V_{ON}$
Regulated Cascode	Good-Excellent	$g_m^2 r_{ds}^3$	$\frac{1}{g_m}$	$V_T + 2V_{ON}$ (min. is $2V_{ON}$ )	$V_T + V_{ON}$ (min. is $V_{ON}$ )

**Summary of BJT Current Mirrors**

Current Mirror	Accuracy	Output Resistance	Input Resistance	Minimum Output Voltage	Minimum Input Voltage
Simple	Poor	$r_o$	$\frac{1}{g_m}$	$V_{CE(sat)}$	$V_{BE}$
Cascode	Excellent	$\beta_F r_o$	$\frac{2}{g_m}$	$V_{CE(sat)} + V_{BE}$	$2V_{BE}$
Wide Output Swing Cascode	Excellent	$\beta_F r_o$	$\frac{1}{g_m}$	$2V_{CE(sat)}$	$V_{BE}$
Self-biased Cascode	Excellent	$\beta_F r_o$	$R + \frac{1}{g_m}$	$2V_{CE(sat)}$	$V_{CE(sat)} + V_{BE}$
Wilson	Poor	$\beta_F r_o$	$\frac{2}{g_m}$	$V_{CE(sat)} + V_{BE}$	$V_{CE(sat)} + V_{BE}$
Regulated Cascode	Good-Excellent	$\beta_F r_o$	$\frac{1}{g_m}$ or less	$V_{CE(sat)}^*$	$V_{CE(sat)}^*$

\* One can design the regulated cascode so that effectively the minimum value of  $V_{MIN}$  (out) is just  $V_{CE(sat)}$ .