Reduction of Transistor Slope Impedance Dependent Distortion in Large-Signal Amplifiers*

MALCOLM HAWKSFORD

University of Essex, Department of Electronic Systems Engineering, Colchester CO4 35Q, UK

0 INTRODUCTION

The static characteristics of a bipolar transistor reveal that, under large-signal excitation, there are sources of significant nonlinearity. In an earlier paper [1] consideration was given to the I_E/V_{BE} nonlinearity, where a family of techniques was presented to attempt local correction of this error mechanism. However, the collector–emitter and collector–base slope impedance of transistors also result in significant distortion, where under large-signal conditions they can become a dominant source of error [2].

The static characteristics show only part of the problem; a more detailed investigation reveals capacitive components which are dependent upon voltage and current levels. Consequently under finite-signal excitation, modulation of the complex slope impedances results in dynamic distortion. It will be shown that the level of error that results from slope distortion is not strongly influenced by negative feedback once certain loop parameters are established. Also, because of the frequency and level dependency of slope distortion, the overall error will contain components of both linear and nonlinear distortion that are inevitably linked to individual device characteristics. It is therefore anticipated that a change of transistor could, in principle, lead to a perceptible change in subjective performance, even when the basic dc parameters are similar.

In this paper consideration is given to a class of voltage amplifiers employing a transconductance gain cell g_m, a gain-defining resistor R_g, and a unity-gain isolation amplifier, together with an overall negative-feedback loop. This structure is typical of most voltage and power amplifiers. However, although it is more usual to focus attention on input stage and output stage distortion, we shall consider in isolation the distortion due only to slope impedance modulation and assume other distortions are controlled to an adequate performance level. It will be demonstrated that significant distortion results from slope modulation, and a design methodology is presented to virtually eliminate its effect, even when the slope parameters are both indeterminate and nonlinear and when signals are of substantial level.

We commence our study by investigating the role of negative feedback as a tool for the reduction of slope distortion and to show that although effective, in isolation, it is not an efficient procedure.

1 NEGATIVE FEEDBACK AND THE SUPPRESSION OF SLOPE IMPEDANCE DEPENDENT DISTORTION

Consider the elementary amplifier shown in Fig. 1, where the principal loop elements are transconductance g_m, gain-defining resistor R_g, and feedback factor k. The nonideality of the transconductance cell is represented by an output impedance Z_n, where ideally $Z_n = \infty$, but in practice is finite and signal dependent. (Any linear resistive component of Z_n is assumed isolated and lumped with R_g.) In general, Z_n is a composite of the slope parameters of the output transistors in the transconductance cell. It can also include a reflection of any load presented to the amplifier. However, we assume here a perfect unity-gain buffer amplifier to isolate the slope distortion of the transconductance cell.

Although Z_n is signal dependent, our analysis will assume small-signal linearity so that performance sensitivity to Z_n can be established. However, the circuit topologies presented in Sec. 3 are not so restricted and can suppress the nonlinearity due to Z_n modulation.

For a target closed-loop gain γ there is a continuum of k and R_g for a given g_m, where the target closed-loop gain γ for $Z_n = \infty$ is defined,

$$\gamma = \frac{g_m R_g}{1 + k g_m R_g} . \tag{1}$$

Hence for a given k, g_m, and γ, R_g is expressed as

$$R_g = \frac{\gamma}{g_m(1 - \gamma k)} \tag{2}$$

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where, for $0 \leq k \leq 1/\gamma$, then $\gamma/g_m \leq R_g \leq \infty$.

The actual closed-loop gain A, for finite Z_n, is

$$A = \frac{g_m Z_n R_g}{Z_n + R_g + k g_m Z_n R_g} \tag{3}$$

and eliminating R_g defined by Eq. (2) for selected target gain γ and transconductance g_m,

$$A = \frac{g_m Z_n}{1 + Z_n g_m/\gamma} . \tag{4}$$

This result demonstrates that the dependence of the transfer function A on Z_n is independent of the selection of feedback factor k, provided the condition of Eq. (2) is satisfied to set the target gain γ.

The error contribution due to Z_n can be estimated by evaluation of the transfer error function [3], [4] E defined by

$$E = \frac{A}{\gamma} - 1 \tag{5}$$

where E represents the ratio of error signal to primary signal and can be visualized according to Fig. 2.

Substituting A from Eq. (4) into Eq. (5),

$$E = \frac{-\gamma}{\gamma + g_m Z_n} . \tag{6}$$

In practice $g_m Z_n >> \gamma$ for a well-behaved amplifier, whereby

$$E \simeq \frac{-\gamma}{g_m Z_n} . \tag{7}$$

The results of Eqs. (6) and (7) reveal that to reduce the dependence on slope distortion, the product $\{g_m Z_n\}$ must increase. However, it is important to observe that Z_n reduces with increasing frequency due to device capacitance and that g_m also reduces with frequency due to closed-loop stability requirements, so that there are fundamental constraints on the effectiveness of slope distortion reduction using overall negative feedback, particularly at high frequency.

As an aside we are assuming g_m to be linear. In practice a reduction of R_g places a heavier current demand on g_m; thus a greater distortion contribution from g_m is to be anticipated for a given output [1]. Also, in power amplifier circuits, the output stage will exhibit distortion under load, a factor not considered in the present discussion. However, the independence of E on k and R_g for a given γ and g_m is true for distortion resulting only from Z_n, and when considered in isolation, it is an interesting example of a distortion that is not reduced by moving from a zero-feedback to a negative-feedback topology, especially as the choice of R_g is often the principal distinction between low-feedback and high-feedback designs [5].

In the next section the common-emitter amplifier is examined as a transconductance cell and current mirror, and an estimate is made of the output impedance Z_n for a range of circuit conditions.

2 OUTPUT IMPEDANCE OF COMMON-EMITTER AMPLIFIER

The common-emitter amplifier is shown in Fig. 3 in both single-ended and complementary formats. In this section the output impedance of the common-emitter amplifier is analyzed in terms of the small-signal parameters for a range of source resistances R_s and emitter resistances R_E. For analytical convenience, the base and emitter bulk resistances are assumed lumped with R_s and R_E, respectively.

Fig. 4 illustrates a small-signal transistor model of the common-emitter cell, where z_{ce} and z_{cb} represent collector–emitter and collector–base slope impedances, respectively, and h_{fe} is the collector–base current gain.

The output impedance Z_c observed at the collector of the common-emitter cell is given by

$$Z_c = \frac{v_o}{\alpha i_o} = \frac{1}{\alpha}\left\{z_{ce} + R_E + \frac{z_{ce}}{z_{be}}[R_E + R_s(1 - \alpha)](1 + h_{fe})\right\} \tag{8}$$

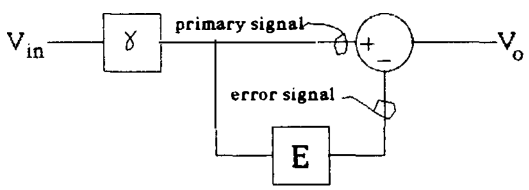


Fig. 2. Transfer error function model of voltage amplifier in Fig. 1.

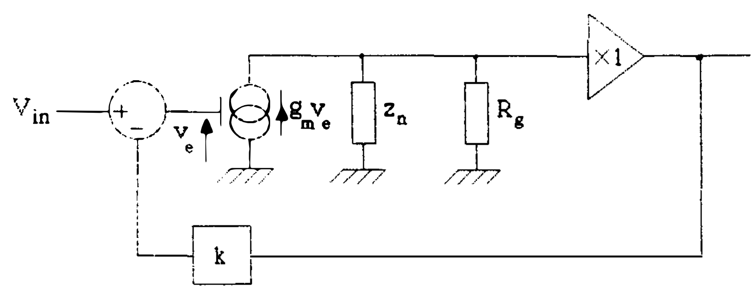


Fig. 1. Elementary amplifier topology using transconductance cell and gain-defining resistor.

where the collector/emitter current division factor is

$$\alpha = 1 + \frac{z_{be}z_{ce} + R_E\lambda}{z_{be}z_{cb} + R_s\lambda} \tag{9}$$

and

$$\lambda = (1 + h_{fe})z_{ce} + z_{cb} + z_{be} \tag{10}$$

or, alteratively, eliminating α,

$$Z_c = \frac{(z_{ce} + R_E)(z_{be}z_{cb} + R_s\lambda) + (1 + h_{fe})z_{ce}(R_E z_{cb} - R_s z_{ce})}{z_{be}(z_{cb} + z_{ce}) + \lambda(R_s + R_E)} . \tag{11}$$

The expressions for Z_c reveal significant complexity, which is compounded by the signal dependence of the small-signal parameter set $\{z_{ce}, z_{cb}, z_{be}, h_{fe}\}$.

To simplify the results, consider a family of approximations for Z_c for specific cases of R_s and R_E, so that the dominant contributors to the output impedance can be determined.

1) *Case 1*: $R_s = 0$, $R_E = 0$.

Eq. (11) reduces to

$$Z_c \simeq \frac{z_{ce}z_{cb}}{z_{ce} + z_{cb}} \tag{12}$$

that is, Z_c is parallel combination of z_{ce} and z_{cb}.

2) *Case 2*: $R_s = 0$, $R_E >> z_{be}/(1 + h_{fe})$.

Eq. (10) approximates to $\lambda = (1 + h_{fe})z_{ce}$ and the denominator of Eq. (11) reveals $\lambda R_E >> z_{be}(z_{cb} + z_{ce})$. Hence,

$$Z_c \approx z_{cb} . \tag{13}$$

This case is typical of the current source and grounded-base amplifier as used in the cascode configuration.

3) *Case 3*: $R_s >> z_{be}$, $R_E = 0$.

From Eq. (11),

$$Z_c \simeq \frac{z_{cb}}{\frac{z_{cb}}{z_{ce}} + \frac{z_{be} + (1 + h_{fe})R_s}{z_{be} + R_s}} \tag{14}$$

where, for $R_s >> z_{be}$, Z_c is z_{ce} in parallel with $z_{cb}/(1 + h_{fe})$ and represents the worst-case output impedance condition.

4) *Case 4*: $R_s >> z_{be}$, $R_E >> z_{be}/(1 + h_{fe})$.

Applying inequalities to Eq. (11), and noting $z_{be} << z_{ce}, z_{cb}$,

$$Z_c \approx \left[\frac{z_{ce}\,z_{cb}}{(1 + h_{fe})z_{ce} + z_{cb}}\right]\left[\frac{R_s + (1 + h_{fe})R_E}{R_s + R_E}\right] + \frac{R_sR_E}{R_s + R_E} . \tag{15}$$

In selecting a circuit topology it should be noted that $z_{cb} > z_{ce}$; thus the grounded-base stage as used in the cascode will offer superior results in terms of output impedance. Nevertheless, z_{cb} is still signal dependent and represents a significant distortion mechanism where large signals are encountered, especially as z_{cb} falls with frequency. Such distortion is demonstrated in Sec. 5.

In Sec. 4 a new form of distortion correction is proposed that reduces output impedance dependence on both z_{ce} and z_{cb} even when nonlinear, and results in lower overall distortion that is virtually frequency independent.

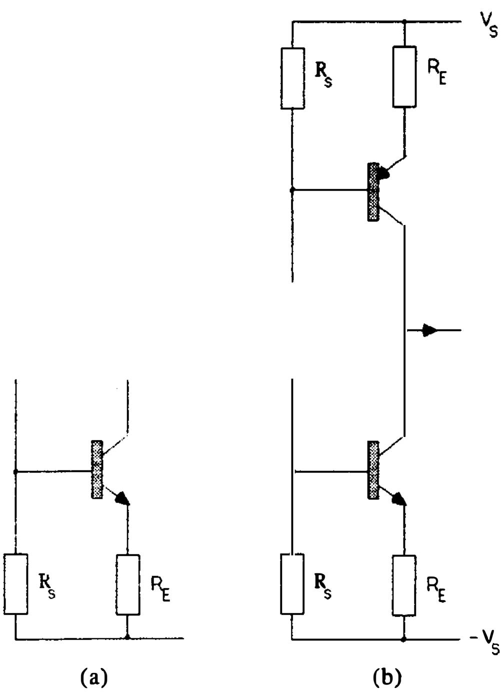


Fig. 3. Common-emitter gain cells. (a) Single-ended current mirror. (b) Complementary current mirror.

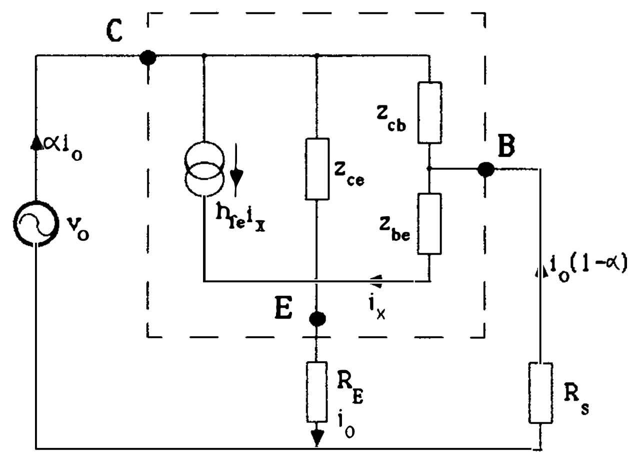


Fig. 4. Small-signal model of common-emitter amplifier showing slope impedances z_{ce} and z_{cb}.

3 REDUCTION OF NONLINEAR SLOPE IMPEDANCE DEPENDENT DISTORTION

The output impedances of the grounded-base and common-emitter amplifier cells are bounded by the device slope impedances z_{cb} and z_{ce}, respectively, as demonstrated by cases 2 and 3 in Sec. 2. However, an examination of Eq. (8) reveals that the factor α in the denominator restricts the output impedance. If a modified circuit topology could be realized such that the base current is summed with the collector current but without incurring an extra load on the collector, then the expression for collector output impedance would become

$$Z_{cu} = \frac{v_o}{\alpha i_o + (1 - \alpha) i_o} = \frac{v_o}{i_o} .$$

Hence from Eqs. (8)–(10) an upper bound on Z_{cu} is established where

$$Z_{cu} = R_E + z_{ce} + \frac{(1 + h_{fe}) z_{ce}(z_{cb} R_E - z_{ce} R_s)}{z_{be}\, z_{cb} + R_s \lambda} . \qquad (16)$$

An examination of Eq. (16) reveals that, with typical component values and transistor parameters, a substantial increase in collector impedance is possible and that this is achieved even when z_{ce} and z_{cb} are dynamic. However, this result is an upper bound that assumes that all the base current is returned to the collector. In practical topologies this is compromised by a small margin, so that lower values should be anticipated.

Two circuit approaches have been identified to meet the requirement of base and collector current summation without direct connection to the collector. These are based on a local feedforward and feedback strategy, respectively, and can be used independently or compounded to give further enhancement.

3.1 Feedforward Topology

The feedforward topology is a derivative of the Darlington transistor that is occasionally employed in power amplifier current mirrors [6], [7]. In Fig. 5 two circuit examples are presented which yield similar performance. In each circuit the base current of the output device is returned to the emitter via the emitter–collector of the driver stage. Consequently the advantages of the Darlington are retained, yet with an enhanced output impedance realized by removing the respective currents in z_{ce} and z_{cb} from the output branch of the complementary stage. It should be noted that the collector–emitter voltage variation of the drivers is small, with only the output collectors swinging the full range of output voltage. The conventional Darlington connection of parallel collectors compromises this ideal, with the driver stage adding a degree of slope distortion under large-signal excitation. It is, however, important to note that a small fraction of output transistor base current is not returned to the emitter and is dependent on the ratio of R_E to transistor output impedance as seen at the emitter of the output device. This fractional loss of current will lower the bound suggested by Eq. (16), although there is still substantial advantage.

3.2 Feedback Topology

The conventional cascode as illustrated in Fig. 6(a) offers an output impedance approaching z_{cb}, which is a significant improvement over the common-emitter stage as $z_{cb} > z_{ce}$. A simple modification to the basic circuit can return the base current of the grounded-base stage to the emitter of the common-emitter stage. Consequently signal current flowing in both z_{ce} and z_{cb} now form local loops which do not include the output branch. The new topology is shown in Fig. 6(b), while in Fig. 6(c) the basic current paths are illustrated which apply even when z_{ce} and z_{cb} are nonlinear. Again, it is only the output device whose collector is required to swing over the full output voltage; thus the common-emitter stage offers a minimal slope distortion contribution.

In circuit applications where the common-emitter stages operate at a high bias current to improve I_E/V_{BE} linearity, a bypass current I_x [see Fig. 6(b)] can lower the operating current of the common-base stage. This technique both reduces output device power dissipation and aids a further increase in the slope impedances, while circuit symmetry ensures that noise in I_x does not flow in the output branch. As a practical detail, experimentation has revealed the desirability of ac bypassing of the base bias resistance of the grounded-base stages [see capacitors C in Fig. 6(b)]. This both enhances circuit operation and eliminates any tendency toward high-frequency oscillation due to the positive-feedback loop formed by the base–emitter connections.

3.3 Compound Feedback/Feedforward Topologies for z_{ce}, z_{cb} Reduction

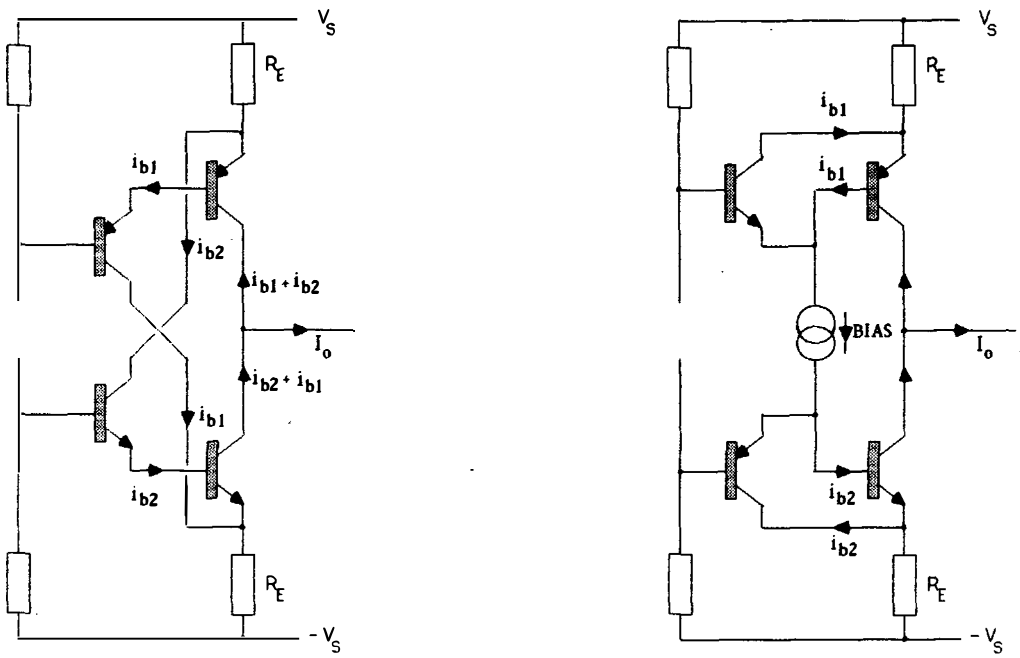
The methods based on feedforward and feedback addition of the output device base current can be compounded to offer further performance advantage. There are many possible topologies offering minor variations, though each uses the same basic concept. It is not intended to analyze each variant, though a family of topologies is presented in Fig. 7 to stimulate development.

4 NOISE CONTRIBUTION OF GROUNDED-BASE STAGE WITH BASE CURRENT SUMMATION

In this section brief consideration is given to the contribution of noise from the common-base stage in the cascode for the two basic topologies shown in Fig. 8.

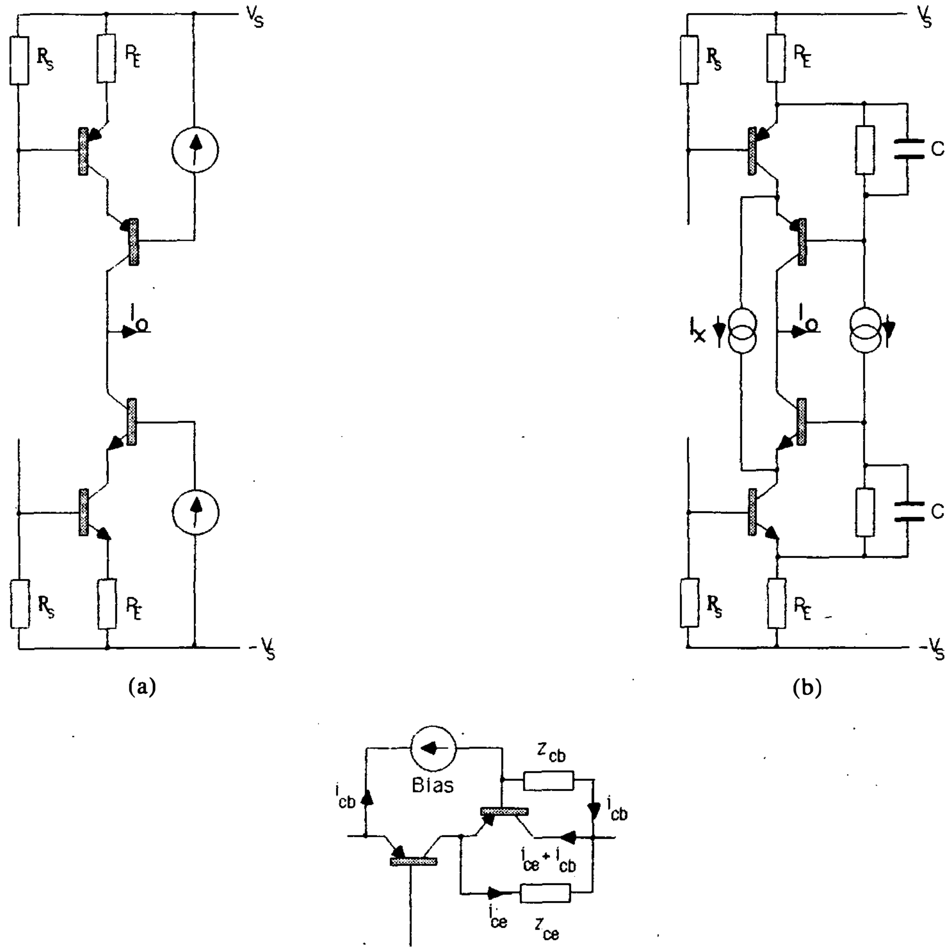
In both cases let $\overline{i_{cn}^2}$ be the mean square noise current in the collector of the common-emitter stage and let the common-base stage have respective noise voltage and noise current sources $\overline{e_n^2}$ and $\overline{i_n^2}$.

It is clear that because the common-emitter stage offers a relatively high output impedance at the collector, the equivalent voltage noise generator of the common-base stage yields a negligible contribution to the output



(a) (b)

Fig. 5. Two examples of feedforward addition of output stage base currents using a two-stage topology. (Observe base current paths i_{b1} and i_{b2}.)



(c)

Fig. 6. Slope distortion reduction using feedback topology. (a) Conventional cascode. (b) Enhanced cascode. (c) Illustration of signal current paths i_{ce}, i_{cb} in z_{ce}, z_{cb}.

noise current.

However, an inspection of the noise current paths reveals that in Fig. 8(a) almost all $\overline{i_n^2}$ must flow in the collector, hence effective load, while in Fig. 8(b) virtually all the noise current circulates locally through the common-emitter stage, resulting in only a fraction, $\approx \overline{i_n^2}/[1 + 1/h_{fe} + h_{fe}R_E/(R_s + R_E + z_{be})]^2$, appearing in the collector (assuming similar transistor h_{fe}'s). Consequently with the enhanced topology there is virtually no extra noise generated by the addition of the common-base stage. Hence the output noise current is also $\overline{i_{cn}^2}$.

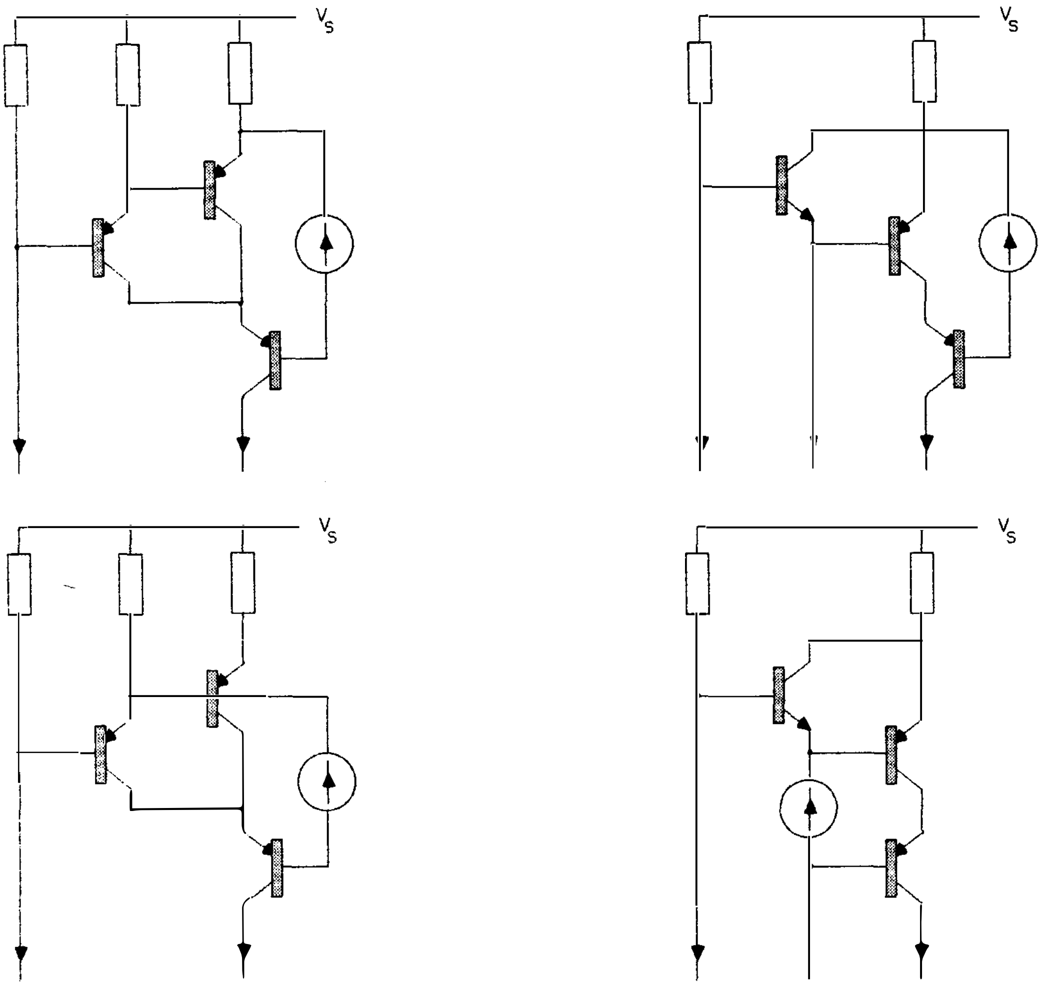


Fig. 7. Circuit examples using two-stage common-emitter amplifier with a common-base output stage.

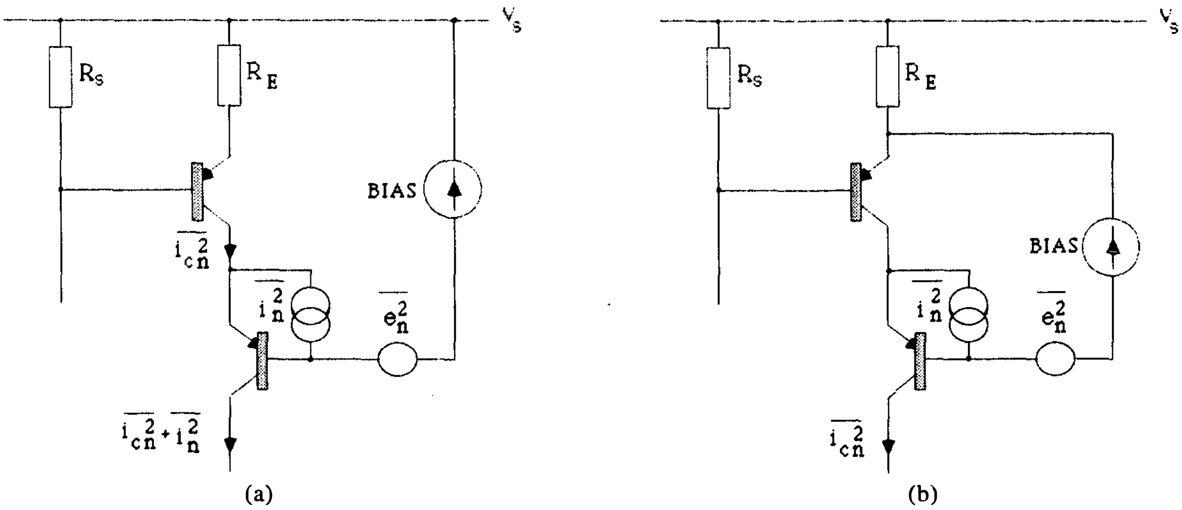


Fig. 8. Noise sources of common-base stage. (a) Conventional cascode. (b) Enhanced cascode.

5 MEASURED PERFORMANCE ADVANTAGE OF ENHANCED TOPOLOGY

To highlight the performance advantage of the modified common-base stage and to demonstrate the significance of slope distortion at large signal levels, a test circuit was constructed to validate the technique and to permit an objective assessment.

Three variants of the circuit were constructed and tested with ascending levels of modification. The enhanced topology is shown in Fig. 9(c), with the comparative output stage variants highlighted in Fig. 9(a) and (b). The circuit is dc coupled and no overall feedback is used. The output voltage is derived using a 10-kΩ gain-defining resistor R_g, and an offset-null potentiometer is provided since no servo amplifier is used. The total harmonic distortion results are given in Table 1. All measurements were performed with a sinusoidal input and an output voltage of 80 V peak to peak.

The results show that the basic circuit exhibits a distortion rising with frequency, reaching an unacceptable 1.9% at 50 kHz. This result is a function of the voltage-dependent nature of the device capacitance and represents a severe dynamic distortion. The conventional cascode exhibits a marked improvement, which reflects the popularity of this topology, where distortions are consistently reduced by 20 dB compared with the no-cascode circuit. However, although distortion products are of a lower order, they are still frequency dependent. This difference in performance arises from the basic common-emitter stage having an output impedance $\approx z_{ce}$, while the common base stage is z_{cb}, where $z_{cb} > z_{ce}$, though they follow the same basic frequency dependence, hence the tracking of the distortion figures.

However, the enhanced cascode, where performance is almost independent of both z_{ce} and z_{cb}, shows a distortion reduction greater than 40 dB at 50 kHz with a very desirable 31.8-dB improvement at 1 kHz over the basic circuit. Of particular significance is the almost frequency-independent nature of the distortion, together with the indication that the two stages of amplification are of inherent low distortion, though clearly they are a limit to linearity for the enhanced circuit. This performance level was masked by slope distortions in the conventional circuit.

These tests are sufficient to validate the technique, especially as the cost overhead is minimal compared with the conventional cascode, and represent a substantial performance enhancement irrespective of whether overall feedback is contemplated in a final design.

6 CONCLUSION

This paper has presented a method of reducing the performance dependence on transistor collector–emitter and collector–base slope impedance parameters, whereby useful distortion reduction can be achieved for large-signal voltage amplifiers.

A theory was presented to demonstrate that for a given input cell transconductance and closed-loop gain, the error signal due to the modulation of output impedance Z_n was not dependent on the level of feedback, provided g_m and target gain γ remained constant. Consequently for the test circuits of Section 5, if overall feedback was applied together with an appropriate increase in the gain-defining resistor R_g, the same level of distortion due to modulation of Z_n should be anticipated. (Note that a unity-gain buffer amplifier would be required.) However, if R_g is raised, the signal current level operating in the transconductance gain stage will fall, resulting in a reduced distortion from modulation in g_m. This later distortion would be particularly evident with the enhanced cascode, where modulation of g_m is now the limiting distortion mechanism.

The enhanced topology has specific application in large-signal voltage amplifiers and, with appropriate circuit additions, to power amplifiers. In particular, MOSFET power amplifiers can benefit by using a more optimum current source to drive the output stage since this reduces dependence on both gate-to-source voltage errors as well as slope impedance modulation errors [8].

A third area of application is RIAA disk preamplifiers that use a transconductance cell and a passive equalization-defining impedance [9], [10]. The more optimum current source will lower distortion and increase EQ accuracy as the current source exhibits a lower output capacitance, together with a higher output resistance, the latter particularly affecting low-frequency performance.

It is interesting to observe that if negative feedback alone were used to reduce error dependence on Z_n by the same factor as the enhanced cascode, at 1 kHz an increase in loop gain of more than 30 dB is required, or at 50 kHz this requirement rises to more than 40 dB. Such factors are often impractical to achieve, thus vindicating the adoption of the enhanced topology. However, more fundamentally, the distortion dependence on transistor slope impedance inevitably rises with both frequency and output voltage level, and moves against the loop gain requirement for stability, thus making negative feedback less effectual in suppressing slope-dependent nonlinearity.

The techniques described in this paper should also find application in circuits that require enhanced supply rail rejection. An appendix outlines how slope impedance distortion reduction can improve the performance of voltage/power amplifiers by enhancing the interface between amplifier stages which alternate their signal reference between ground and supply rail.

Although the reduction of large-signal-related errors arising from slope distortion has been the central thesis, the reduction of linear distortion at lower signal levels is also welcome. Slope distortion has been shown to involve several factors that depend on both transistors and the associated circuit elements in a particular application. Such device-specific distortion can, in principle, contribute to the subjective performance and reflects the mutual interrelationship of transistors and circuit construction, which results in small deviations from the target transfer function.

The paper has presented a family of primitive circuit topologies based on the same principle as the enhanced cascode, which are candidates for adoption in transconductance-based amplifiers. There are numerous circuit possibilities for enhancement. However, the two

Table 1. Total harmonic distortion.

Test frequency, kHz	No cascode, %	Conventional cascode, %	Enhanced cascode, %
1	0.39	0.039	0.010
10	0.47	0.11	0.011
20	0.51	0.14	0.012
50	1.9	0.16	0.016

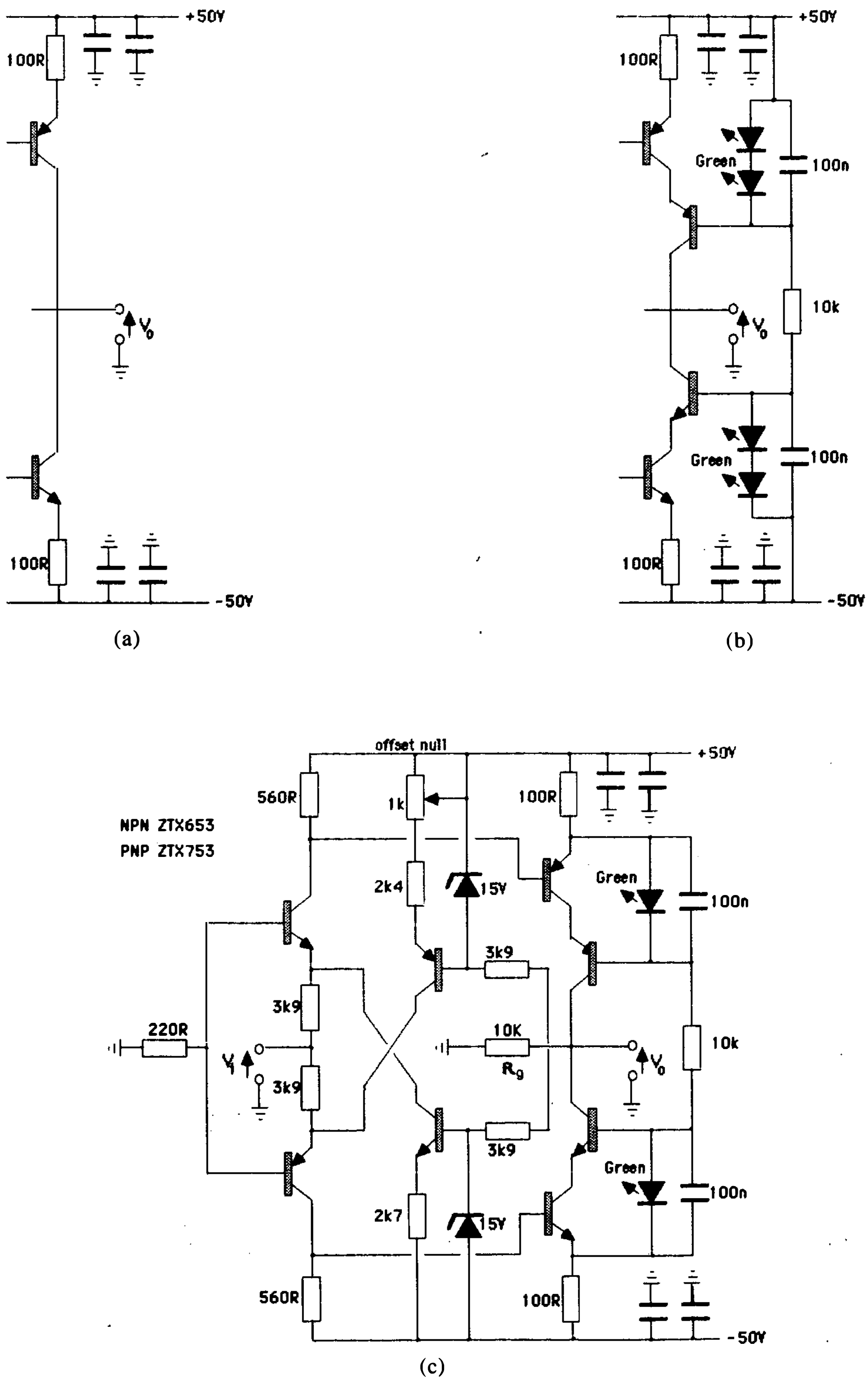


Fig. 9. Test circuit with three output stage variants. (a) Complementary common-emitter output stage. (b) Complementary cascode output stage. (c) Complete test circuit with enhanced cascode.

basic principles to be observed are

1) Adequately high effective emitter resistance R_E to disassociate z_{ce} from the output impedance at the collector;

2) Addition of base current to collector current, without adding extra circuitry to collector, to disassociate z_{cb} from the output impedance at the collector.

Observation of these two principles then enables a transformation of the signal level from low voltage to large voltage without incurring a significant distortion penalty due to dynamic modulation of the transistor slope parameters, together with a distortion characteristic that is considerably less frequency dependent.

7 ACKNOWLEDGMENT

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APPENDIX
SUPPLY RAIL REJECTION AS A FUNCTION OF INPUT STAGE AND CURRENT MIRROR SLOPE IMPEDANCES

In this appendix the sensitivity of a two-stage negative-feedback amplifier is determined as a function of the slope impedances Z_{n1} and Z_{n2} of the two stages. The basic circuit is shown in Fig. 10 where g_m is the transconductance of the input stage, m the current gain of the current mirror, R_g a gain-defining resistor, r_2 the input impedance of the current mirror ($r_2 << Z_{n1}$), and k the feedback factor.

Using linear analysis to express V_o as a function of both V_{in} and V_s,

$$V_o = \frac{mg_mR_gV_{in} + R_g[m/Z_{n1} + 1/Z_{n2} + r_2/Z_{n1}Z_{n2}]V_s}{(1 + r_2/Z_{n1})(1 + R_g/Z_{n2}) + kmg_mR_g} . \tag{17}$$

Let δ be the ratio of output to input transfer functions for inputs V_s and V_{in},

$$\delta = \frac{V_o/V_s}{V_o/V_{in}} \tag{18}$$

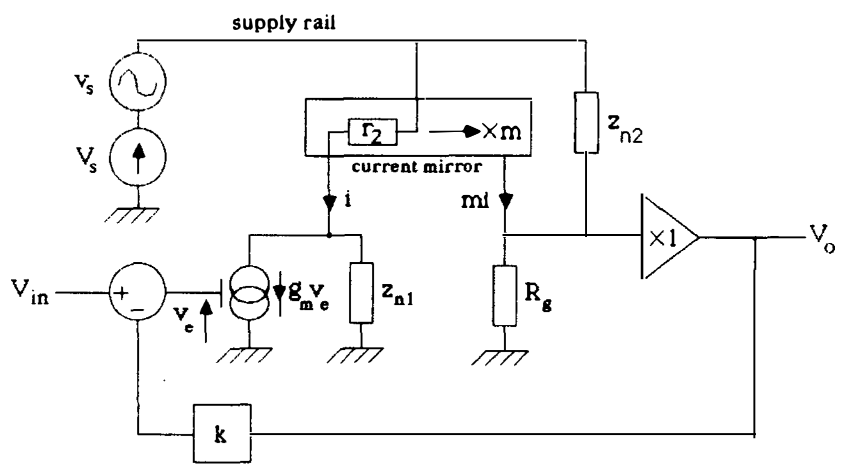


Fig. 10. Two-stage voltage amplifier with v_s representing power supply voltage variation.

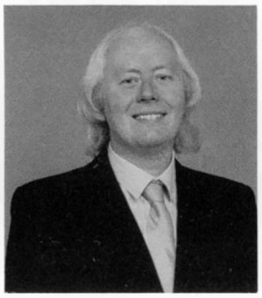
and

$$\delta = \left[\frac{1}{Z_{n1}} + \frac{1}{mZ_{n2}}\left(1 + \frac{r_2}{Z_{n1}}\right)\right]\frac{1}{g_m} . \qquad (19)$$

The results show that the slope impedances define the suppression of supply rail rejection together with g_m. This is particularly important in power amplifier applications, where in class AB operation V_s is wide band (>>20 kHz) and a nonlinear function of the input signal due to output stage commutation. The advantages of maximizing both Z_{n1} and Z_{n2} and using separate power supplies for voltage amplifier and output stage in power amplifiers are evident.

Eq. (19) is also shown to be independent of R_g. However, in high loop gain applications where g_m is large, the high-frequency distortion characteristics together with the falling high-frequency gain of g_m may become a limiting factor, particularly if required to suppress wide-band power supply injection. In low-feedback applications, the slope impedance dependent distortion is suppressed more by the presence of R_g than by the presence of g_m. For example, observe how R_g and Z_{n2} form a potential divider to supply injected distortion, but as $R_g \rightarrow \infty$, the distortion is processed completely by the feedback loop. Also in low-feedback designs greater local feedback enhances the wide-band distortion characteristics of g_m and helps aid an overall distortion profile which is less frequency dependent.

THE AUTHOR



Malcolm Hawksford is a senior lecturer in the Department of Electronic Systems Engineering at the University of Essex, U.K., where his principal interests are in the fields of electronic circuit design and audio engineering. Dr. Hawksford studied at the University of Aston in Birmingham and gained both a First Class Honors B.Sc. and Ph.D. The Ph.D. program was supported by a BBC Research Scholarship where work on the application of deltamodulation to color television was undertaken.

Since his appointment at Essex, he has established the Audio Research Group, where research on amplifier studies, digital signal processing and loudspeaker systems has been undertaken. Dr. Hawksford has had several AES publications that include topics on error correction in amplifiers and oversampling techniques for ADC and DAC systems. His supplementary activities include designing commercial audio equipment and writing articles for Hi-Fi News—activities that integrate well with visits to Morocco and France. His leisure activities include listening to music, motorcycling and motor mechanics. Dr. Hawksford is a member of the IEE, a Chartered Engineer, Fellow of the AES, and a member of the Review Board of the AES *Journal*.