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Ideas for the amplifier with nested Miller compensation

Experience shows that the “sound” of an amplifier may strangely and quite strongly depend on high-frequency effects like the value of snubber capacities around the main rectifiers, the type of these rectifiers or a small change in the unity gain frequency (UGF) or the phase margin of the global feedback loop. I was therefore looking for a topology where each feedback loop spanning more than one transistor should have a UGF of at most 300 kHz, this of course being an arbitrary frequency.

[[Therefore, for the beginning, I also opted for an output stage with single emitter followers, hopefully avoiding problems with instability problems in this stage. (Some High-End manufacturers as e.g. DartZeel follow the same way …) For my low-power amplifier with 20 V supply voltages and D44/D45 output transistors, a quiescent current of 50 mA in both output and “VAS” is sufficient.]]

At a first glimpse, the low UGF seems to exclude any high negative feedback (NFB) around the amplifier output stage at, say, 20 or 40 kHz. Johan Huijsing's excellent book “Operational Amplifiers – Theory and Design” discusses some variants of nested Miller compensation. In his variants, each additional feedback loop has to have a UGF being at least a factor two lower than the already existing loop. This would result in a phase margin of 60 degree for each additional loop. If we have e.g. an “inner” loop with UGF 300 kHz, than an additional loop “outer” would only allow an UGF of 150 kHz – already less than 20dB additional NFB at 20 kHz.

This effect is shown in schematics 1 and 2, schematic 1 sketching the “standard architecture” with single Miller compensation. The whole amplifier shall have a gain of 11. Stage E1 is the emitter follower output, E2 is the mostly so-called “voltage amplifier stage” VAS, and G1 is the differential input stage. The global NFB loop including the output stage has an UGF of 300 kHz, the loop around the “VAS” is somewhat undefined, because its UGF and phase margin depend on the characteristics of the used transistor and the loading by the output stage. In schematic 2, an additional stage G2 has been added. Its gm is only 0.18 mA/V, because its input is at high frequencies directly connected to the output, whereas in schematic 1 we had additionally the feedback network between output and stage input. Now, both Miller loops nominally would have a UGF of 300 kHz, but the outer loop in fact has a lower UGF. We could correct that by increasing its gm to 3 mA/V, but the problem of the low phase margin tending to 45 degrees remains. If we reduce the gm of G1 to 1.2 mS, we obtain an UGF of around 150 kHz and a phase margin of around 60 degree. This is the “standard way” for nested Miller compensation in operational amplifiers (Huijsing's book), where additional and high-accuracy passive elements are to be avoided.

Can we do better? The first step is to include a resistor in series with the outer Miller capacity (schematic 3, R1). If we choose it in such a way that it introduces a “zero” (in the transfer function for the outer next, here the global, loop) exactly at the UGF of the inner loop, than both loops can have the same UGF, and the outer loop again has a phase margin of around 90 degrees! This is the key to add more Miller loops without reducing the UGF and therefore the gain in NFB and without reducing the phase margin (both of course only in principle).

For an implementation, however, we have a problem. Our implementation for G2 will have an input capacitance, forming an additional low-pass together with R1. In the example, this additional pole would be too low to be neglected. We could reduce R1 and increase both C2 and gm of G1. This is possible if G1 can deliver enough current to load and unload C2; otherwise we end up with an amplifier of low slew rate. Another solution is sketched in schematic 4. We connect the Miller capacity to a reduced version of the signal from OUT. This allows to increase C2 and reduce the additional resistor (now effectively formed by (R4 || R5) + R1), but both gm and current delivery of G1 can remain the same. C2 grew by a factor of ten, but in order to achieve a certain voltage swing

at OUT, it only needs to be charged to one tenth of the swing.

In order to allow recursive application of this principle, we need a simple and therefore fast implementation of G2 and possibly further stages (G1 remains the standard differential input stage). The version used is sketched in schematic 5. It is not differential, and therefore cannot deliver ultra-low distortion – the last order of magnitude of distortion reduction has to be realised with a (or possibly two Miller-nested) symmetrical gain stage(s). The gm is given by R1 (plus emitter resistances of Q1 and Q2), and C1 provides a handy means to correct a high-frequency loss of phase margin. With this principle and simple BC550/60 transistors, we were able to nest as much as 5 Miller loops, each having a UGF of 300 kHz, a phase margin of around 90 degrees, and a gain margin of more than 20 dB.

At the stage directly before the “VAS”, one can replace the current source I1 by a resistor, here base to emitter of the “VAS” transistor. A current source does not bring much benefit, since the small-signal input resistance of the “VAS” is quite low. (This changes, however, if we add the usual resistor for current sensing at the “VAS” emitter.) Additionally, Q2 can serve for free as level-shifter to a stabilised, low-noise voltage supply for the small-signal stages.

A practical DIY-advantage of the whole principle lies in the fact that one can start breadboarding with a “standard architecture” and subsequently add more and more intermediate Miller loops. Thus, one can build up the complex schematic step-by-step, checking operating points, stability and frequency response with each step.

Open Problems

At this quality level we should avoid a speaker relay. Without additional circuitry, the amplifier output will shortly swing to full supply voltages during turn-on and turn-off. It turns out that turning on the amplifier in a civilised way is not simple because it is only conditionally stable. If the small-signal stages oscillate with full amplitude into saturation, then the nice gain and phase margins from small-signal analysis with stable operating points do not help at all.

Until now, I have a preliminary solution that reduces swing at turn-on to around +/-1 V (without oscillations/beeps). During turn-off, still some disturbing noise is produced (room-listening level with my relatively inefficient speakers).

Clipping behaviour is horrible. Clipping *must* be circumvented.