The Link Between The Phase Margin And The Converter Transient Response

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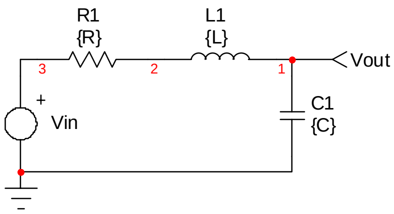
When designing a closed-loop system, a switch-mode power supply for instance, a path is created between the variable you want to monitor and the control pin of your converter. This control pin can be the peak current set point in a current-mode power supply or the duty-cycle input with a voltage-mode controller. If the monitored variable deviates from its imposed target, the controller reacts by either increasing or decreasing the delivered power to the load via an amplified error signal fed to its control pin. The power stage, however, is affected by a gain and a phase that are frequency dependent, *H(s)*. To make sure the resulting power supply will behave per the specified data, it is the designer task to shape the return path *G(s)* to compensate for the power stage response at certain frequency points. Among the important parameters are the dc gain for the smallest static error and the lowest output impedance, but also the cross over frequency for the required response speed. At the cross over point, where the loop gain module *T(s)* equals 1, the returning signal will be affected by a certain phase rotation. If the signal returns in phase with the control signal, we have conditions to form an oscillator, something you want to avoid. To make sure the signal does not return in phase, that is to say with a 360° phase rotation, you must plan a certain amount of margin between the phase rotation of *T(s)* at the cross over frequency and the 360° limit: this is the phase margin. However, how much phase margin should you ask to combine performance and stable answer? 45° as often found in the books, more than that? Let us discover how much through the following lines.

A second order system

Figure 1 shows a *LC* low-pass filter where the resistor *R* illustrates the losses in the network. This architecture could be seen as a simplified lossy output filter of an unloaded buck converter. In that case, the input voltage V_{in} represents the average level of the square wave signal present at the power switch/freewheel diode cathode junction. For the purpose of this study, this average voltage will be ac modulated and we are looking for the expression of the output voltage across the output capacitor. We will then calculate the transfer function *H(s)* = $V_{out}(s)/V_{in}(s)$ of this structure.



parameters

f0=235k
L=10u
C=1/(4*3.14159^2*f0^2*L)
w0=({L}*{C})^-0.5
Q=10
R=1/((({C}/(4*{L}))^0.5)*2*{Q})

Figure 1: a buck converter can be represented by a simple low-pass filter. The script at the bottom automates the calculation of *R* when changing the *Q* value.

Using Laplace notation, (1) describes the transfer function *H(s)* of this *RLC* network:

$$H(s) = \frac{1}{LCs^2 + RCs + 1} \tag{1}$$

By re-arranging the expression, it becomes possible to identify the quality coefficient *Q* and the resonant frequency ω_r.

$$H(s) = \frac{1}{\frac{s^2}{\omega_r^2} + 2\zeta\frac{s}{\omega_r} + 1} = \frac{1}{\frac{s^2}{\omega_r^2} + \frac{s}{\omega_r Q} + 1} \qquad (2)$$

Where, ω_r is the resonant frequency, ζ (zeta) is the damping factor and Q, the quality coefficient:

$$\omega_r = \frac{1}{\sqrt{LC}} \text{ (3) , } \zeta = R\sqrt{\frac{C}{4L}} \text{ (4), } Q = \frac{1}{2\zeta} \text{ (5)}$$

The idea is now to evaluate the response to a 1-V input step and change the quality coefficient values by tweaking the resistor R_1. This resistor is representative of the losses in the network such as the Equivalent Series Resistor of the inductor for instance. As you can read in Figure 1, we have automated the calculation of R whose value is evaluated according to the selected Q. We could also multiply (1) by *1/s* and calculate the inverse Laplace transform to obtain the temporal response. A SPICE simulation will be faster in our case. The results appear in Figure 2.

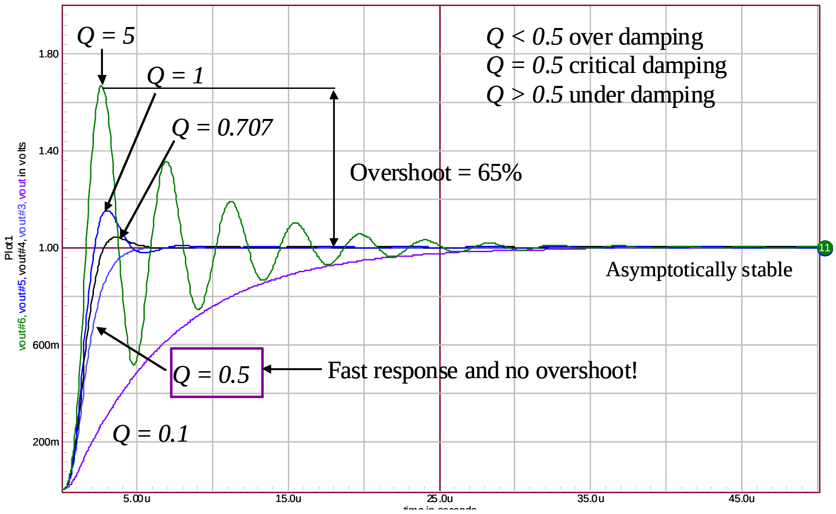


Figure 2: when Q is swept from 0.1 to 5, the answer to a step is either slow (Q = 0.1) but without overshoot or faster, with a large overshoot for big Q values.

As one can see, low Q values lead to a completely oscillation free response whereas values above 0.5 give birth to overshoots. As Q increases, meaning less losses, the overshoot gets larger. If Q would go to infinity, it would imply an undamped LC network keeping oscillations going further to an excitation.

Looking for roots

The study of (2) denominator will reveal the roots for which $H(s)$ goes to infinity. Mathematically, it corresponds to the following characteristic equation:

$$\frac{s^2}{\omega_r^2} + \frac{s}{\omega_r Q} + 1 = 0 \qquad (6)$$

Where the roots come easily as follows:

$$s_1, s_2 = \frac{\omega_r}{2Q}\left(-1 \pm \sqrt{1 - 4Q^2}\right) \qquad (7)$$

In (7), the term under the square root can either be positive or negative, depending on the quality coefficient value. For Q values below 0.5, the so-called *overdamped* case, the term under the square root remains positive and both roots s_1 and s_2 are separated real roots. The step response is sluggish as shown in Figure 2. When Q reaches 0.5, called the *critically damped* case, the roots are still real but are now coincident. The step response is much faster but still does not exhibit overshoot. Now, if Q further grows, we are in an *underdamped* case and the roots welcome an imaginary portion that increases as Q goes up: we have a fast step response now featuring overshoot and oscillations. If Q reaches infinity, the real portion of roots s_1 and s_2 fades away and the system freely oscillates: there is no more damping (losses) brought by the real terms. Analysing the trajectory of these roots is called *root locus analysis*: it shows how the roots are positioned in the s-plane and give indication on how they move in relationship to some parameters. It is Q in this example but it could be the gain k of a system where, at some point when k is increased, the roots migrate in the right half plane and create an instability. Figure 3 describes the path taken by s_1 and s_2 as Q changes.

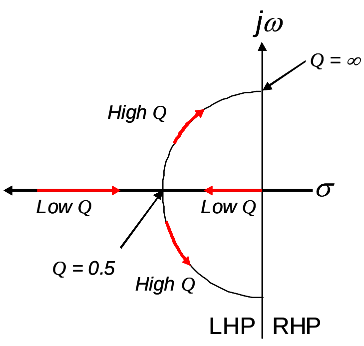


Figure 3: root locus analysis helps to understand how the roots move in relationship to a selected parameter, here the quality coefficient of our *LC* network.

Approximation of an open-loop response

Based on what we have already disclosed, it would be interesting to model our closed-loop dc-dc converter with an equation where a quality coefficient term would appear. That way, we could select the parameter that affects this Q to shape the output response we are looking for: slow but without any overshoot or, on the opposite, faster but accepting a little overshoot. Let us start the derivation process by looking at Figure 4:

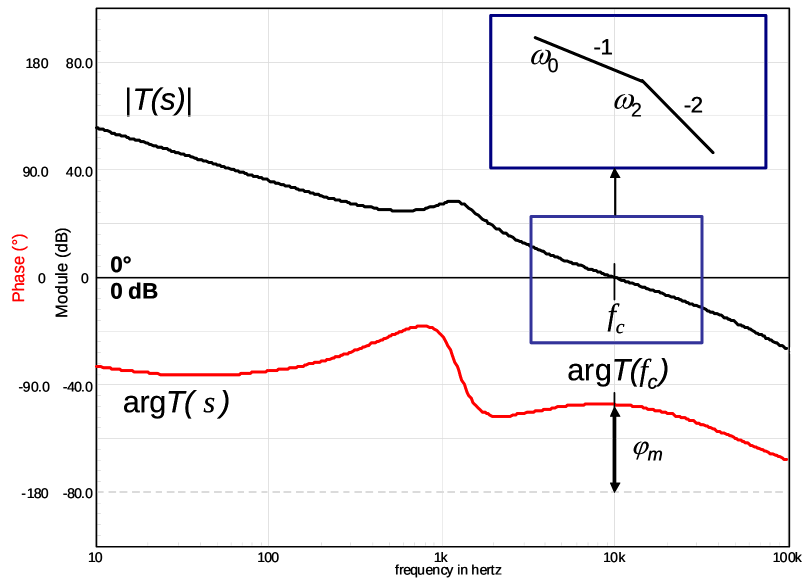


Figure 4: the open-loop response of a compensated buck converter can be approximated to a second-order system in the vicinity of the cross over frequency.

This figure shows the complete loop gain *T(s)* made of the converter power stage transfer function *H(s)* further shaped by the compensator transfer function, *G(s)*. This example is dealing with a CCM buck converter operated in voltage-mode control. In this figure, we concentrate on the area around the cross over frequency f_c which represents one important design parameter of the dc-dc converter you try to stabilize. Asymptotically looking at the curve within the frame reveals the effects of an origin pole ω_0 and a high frequency pole ω_2. Mathematically, this approximation can be formulated by:

$$T(s) \approx \frac{1}{\left(\frac{s}{\omega_0}\right)\left(1+\frac{s}{\omega_2}\right)} \tag{8}$$

In this approximated expression, we consider extra poles and zeros far away from f_c, naturally limiting their impact on the transfer function. However, our interest lies in the response the dc-dc converter is going to deliver once its loop is closed. In other terms, let us identify the closed-loop transfer function derived from (8). To obtain the closed expression, we can evaluate $T(s)/(1+T(s))$:

$$\frac{T(s)}{1+T(s)} = \frac{1}{\frac{s^2}{\omega_0\omega_2}+\frac{s}{\omega_0}+1} \tag{9}$$

Equation (9) appears arranged in form that recalls that of (2). Therefore, we can put it under the familiar form of a second order system as described by (10):

$$\frac{T(s)}{1+T(s)} = \frac{1}{\frac{s^2}{\omega_r{}^2}+\frac{s}{\omega_r Q}+1} \tag{10}$$

The identification of the quality coefficient Q and the resonant frequency ω_r is straightforward: $Q = \sqrt{\frac{\omega_0}{\omega_2}}$ (11) and $\omega_r = \sqrt{\omega_0\omega_2}$ (12).

We now have an equation that describes the approximated closed-loop response of our dc-dc and it includes a quality coefficient. The next step is to establish a relationship between the closed-loop Q and the key design parameter, the open-loop phase margin. First, based on (8), let us calculate the cross over frequency brought by the location of the origin pole ω_0 and its associated high frequency pole ω_2. At the cross over point, we know that the $T(s)$ module equals 1. Therefore:

$$\left|\frac{1}{\left(\frac{j\omega_c}{\omega_0}\right)\left(1+\frac{j\omega_c}{\omega_2}\right)}\right| = 1 \tag{13}$$

Extracting ω_c and re-arranging gives:

$$\omega_c = \frac{\omega_2\sqrt{\sqrt{1+4\left(\frac{\omega_0}{\omega_2}\right)^2}-1}}{\sqrt{2}} \tag{14}$$

If we substitute ((12)) into (14), we obtain a *Q*-dependent cross over frequency :

$$\omega_c = \frac{\omega_2\sqrt{\left(\sqrt{1+4Q^4}-1\right)}}{\sqrt{2}} \tag{15}$$

Equation (15) shows us how the closed-loop quality coefficient and the open-loop cross over frequency are linked. It is important for this remark to be well understood: *Q* represents the resulting closed-loop response quality coefficient based on the open-loop pole/zero arrangement describing the approximated open-loop compensated transfer function *T(s)* in (8).

To continue further with our analysis, we evaluate the phase rotation of *T(s)* at the cross over frequency:

$$\arg T\left(\omega_c\right) = -\left(\tan^{-1}\frac{\omega_c/\omega_0}{0}+\tan^{-1}\frac{\omega_c}{\omega_2}\right) = -\tan^{-1}\frac{\omega_c}{\omega_2}-\frac{\pi}{2} \tag{16}$$

The phase margin φ_m represents the distance between the total phase rotation at the cross over frequency – given by (16) – and the –180° limit. In this case, we purposely neglect the phase reversal brought by the operational amplifier. Hence, we have:

$$\varphi_m = \pi + \arg T\left(\omega_c\right) \tag{17}$$

Substituting (16) into (17), we obtain:

$$\varphi_m = \pi - \tan^{-1}\frac{\omega_c}{\omega_2} - \frac{\pi}{2} = \frac{\pi}{2} - \tan^{-1}\frac{\omega_c}{\omega_2} \tag{18}$$

Remembering our “far far away” trigonometric classes (!), we have:

$$\tan^{-1}x + \tan^{-1}\frac{1}{x} = \frac{\pi}{2} \tag{19}$$

Thanks to (19), we can update (20)(16):

$$\varphi_m = \tan^{-1}\frac{\omega_2}{\omega_c} \tag{20}$$

We have already defined the cross over frequency versus the closed loop quality coefficient in (15). If we capitalize on this definition in (20)
, we have:

$$\varphi_m = \tan^{-1}\left(\sqrt{\frac{2}{\sqrt{\left(1+4Q^4\right)}-1}}\right) \tag{21}$$

The next step is to extract the closed-loop quality coefficient from (21) and simplify the result:

$$Q = \frac{\sqrt[4]{1+\tan\left(\varphi_m\right)^2}}{\tan\left(\varphi_m\right)} = \frac{\sqrt{\cos\left(\varphi_m\right)}}{\sin\left(\varphi_m\right)} \tag{22}$$

This is it! We now have a relationship between our main design criterion the open-loop phase margin and the quality coefficient our loop will exhibit once closed. The best is to explore the various *Q* different phase margin choices will bring though a graph as proposed by Figure 5.

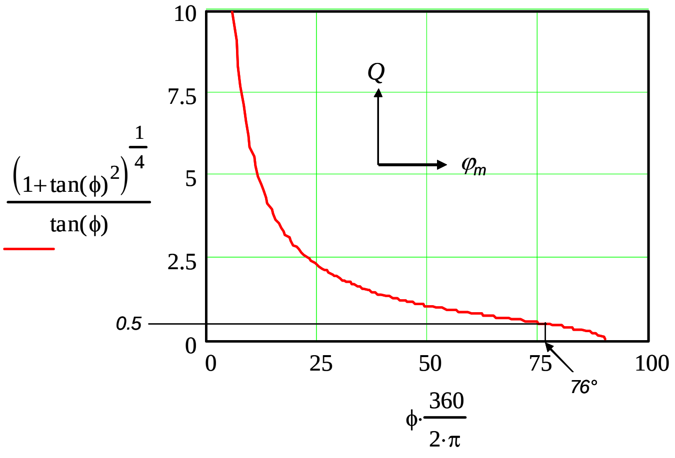


Figure 5: the graph shows the evolution of the closed-loop quality coefficient as you select different phase margin.

If you want to combine speed and lack of overshoot, Figure 2 suggests a *Q* of 0.5. Reading the corresponding phase margin in Figure 5, we can see a design criterion of 76° satisfies this request for such a *Q*, far away from the 45° found in the majority of text books! What does it mean then? In the response to a load step, once the loop is closed, the open-loop phase margin mostly affects the recovery shape and a little the undershoot depth. Therefore, it really depends on the kind of response you are looking for or what the customer specifications impose on your design. If a fast recovery is needed and a little overshoot accepted, then reducing the phase margin can be an option. On the contrary, if absolutely no overshoots are tolerated, you have no choice than increasing the phase margin to the detriment of the recovery speed. Whatever solution you select, you have to make sure that whatever the operating conditions, input/output, temperature and normal parametric variations (ESRs for instance), the phase margin never goes below 45°. In other words, shooting for a typical value around 70° should become a good design practice.

Transient response and phase margin

We have stabilized the buck converter using one of the automated simulation platforms described in Ref. [1]. The technique allows to keep the same cross over frequency while playing on the phase margin only. The overall shape is the same as that presented in Figure 4 with a 10-kHz cross over frequency. The output is subjected to step ranging from 1 A to 2 A in 1 µs. The results appear in Figure 6. The 76° phase margin gives a little overshoot of 0.05% whereas the 49° margin triples that overshoot, still reasonable though given the vertical axis scale of 20 mV per division. However, you can observe a faster recovery in the 49° phase case (70 µs) versus the 76° case (227 µs). Why do we still have overshoot with the 76° when theory states there should be none? It is because (8) is a simplified view of the transfer function in the vicinity of the cross over frequency. As detailed in Ref. [2], if you have three or more poles installed near the cross over frequency, the *Q* factor approximation we have been through does not work anymore and extra work is required. Nevertheless, as exemplified by Figure 6, a small phase margin leads to a peaky closed-loop response.

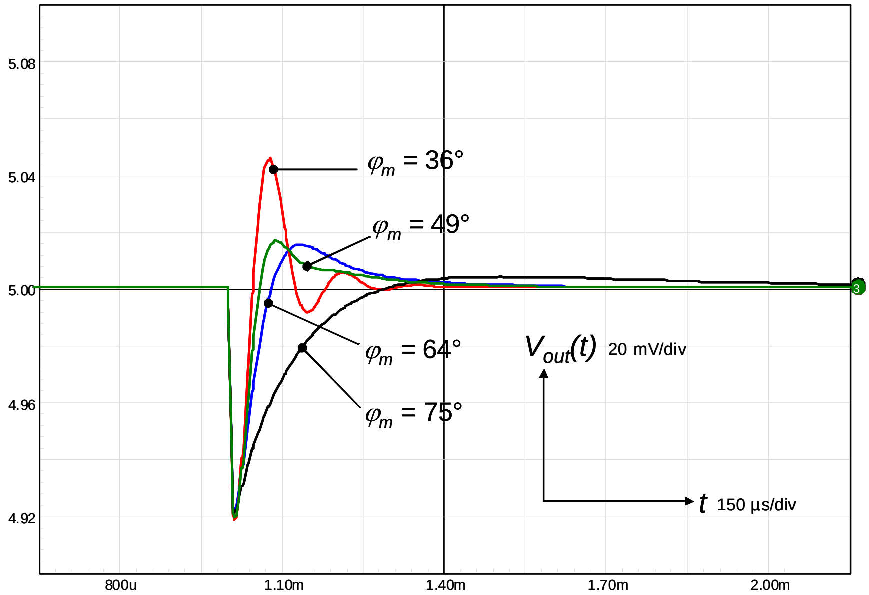


Figure 6: the phase margin has been adjusted at different values and it clearly affects the transient response in both the recovery time and the overshoot above the 5-V target.

Conclusion

The design of a power converter requires cares when it comes to loop control. Numerous text books just recommend to design for a 45° phase margin without any explanations. This article shows how to analytically derive a phase margin target which is surprisingly higher than 45° and close to 76°. Despite some approximations at the beginning of the study, the final result is backed up by simulation results that confirm the need for a phase margin greater than the classical 45° recommendations.

References

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2. R. Erickson, D. Maksimovic, "Fundamentals of Power Electronic", Kluwers Academic Press, 0-7923-7270-0