Review of Marcel's shift register Firdac

After having tested Marcel's solid state Firdac, I was curious to see how it compared to the shiftregister Firdac because of the different conversion method and the separate analogue filter board.
It should be obvious that the Solid State Firdac is meant to be used with PCM coded audio files while the shifregister Firdac has to be used with pure I2S DSD signals, split in Left, Right and Clock .

For splitting the .dsf files into left, right and clock, I used the Amanero Combo384, for which Marcel's board already had a connector available.
With JRiver I could convert .wav files into .dsf files which had to be offered in DoP format to the Amanero board.

In the lossy conversion process from .wav to .dsf, depending on the used SDM strategy, the number of used decimals and rounding strategy some corruption may get added to the original signal.
That could have caused that the THD for 1Khz@0dB and the IMD for 19K+20K@0dB peak were slightly higher as with Marcel's Solid State Dac, but distortion figures were still in the ppm range and can therefore be disregarded.

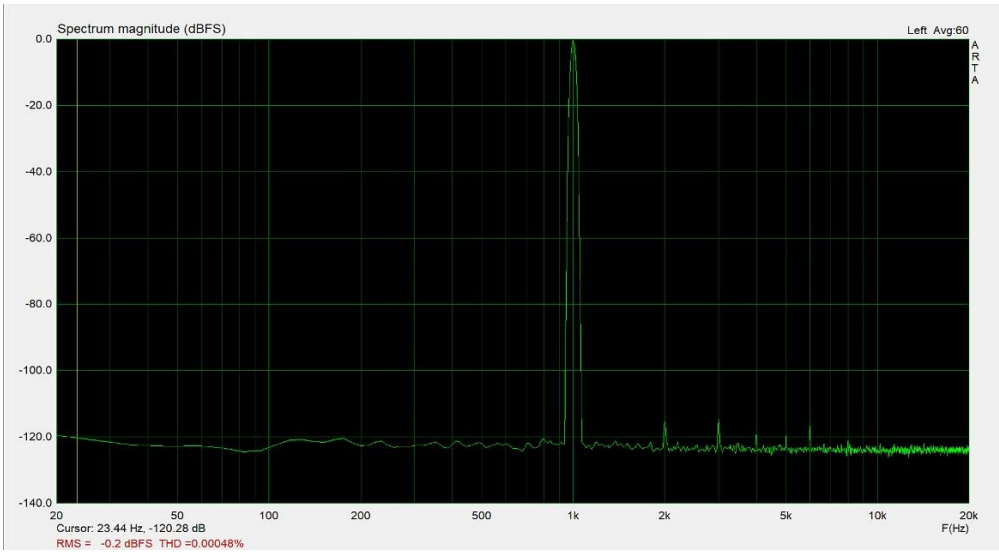

Fig 1, Harmonic distortion at 4.8ppm for 1Khz@0dB

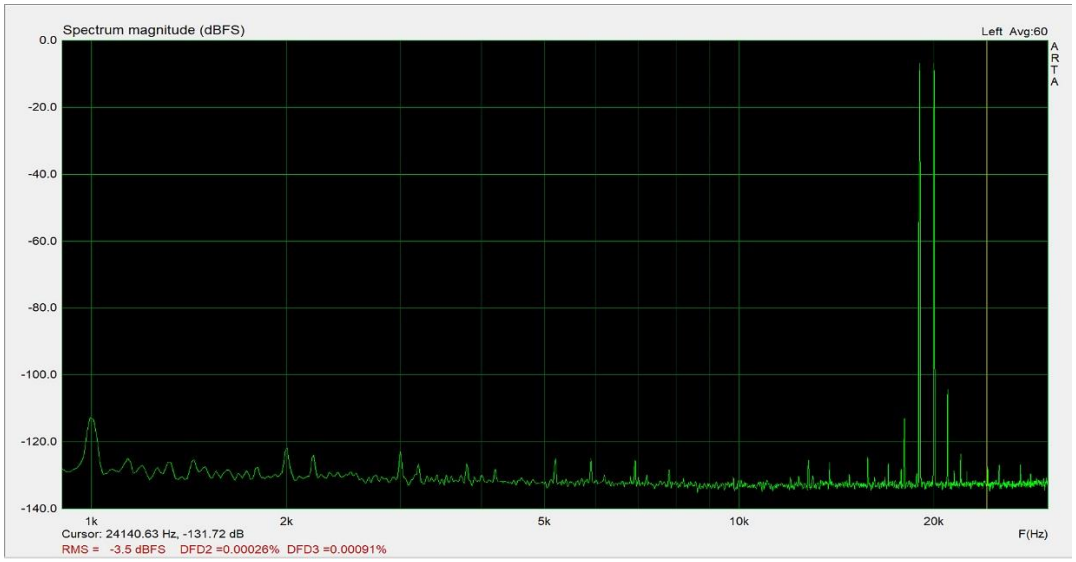

Fig 2, IMD distortion at resp 2.6ppm 2nd order and 9.1ppm 3rd order for 19K+20K at 0dB peak

To measure the various noise signals, I used a 19.5dB gain 0.31nV/rtHz fully differential LNA, dropping to ca. 1.4nV/rtHz when including the two 50R Firdac output resistances and increasing the sensitivity of the measuring chain by 19.5dB.
To calibrate my measurements, I processed a -90.3dB sine at 1Khz, and indeed did it show the 90.3dB sinewave to be at -70.8dB because of the inserted 19.5dB low noise amp's gain.

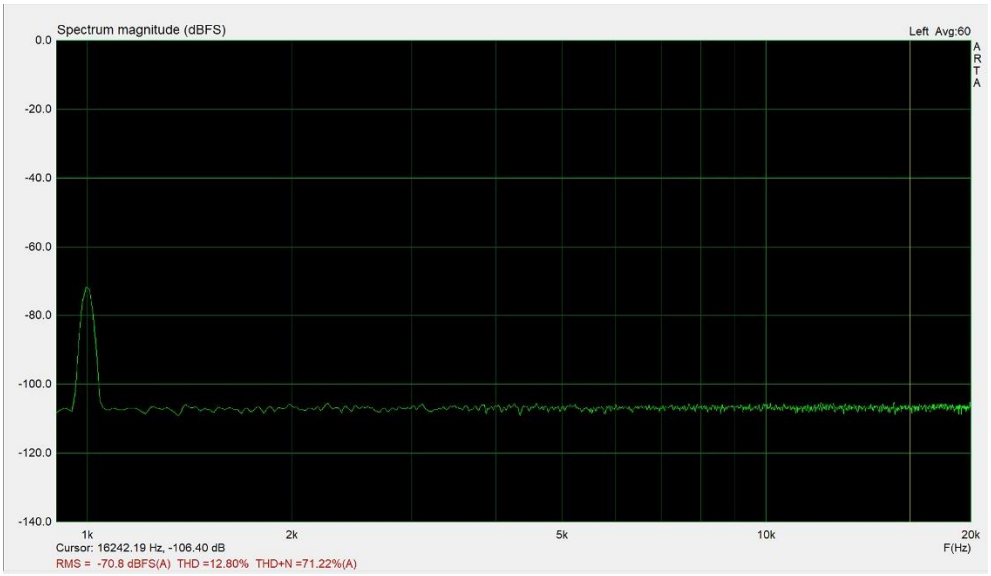

Fig 3, A -90.3dB 1Khz sinewave, amplified by 19.5dB.

Next step was measuring the S/N while using a silent track.
Arta seemed less accurate in doing the noise measurements because of the rather huge out of band noise that seemed to cause aliasing in the audio bandwidth.
After having converted a PCM formatted Silent Track into resp DSD64 up to DSD512, I could produce the image below, showing the Firdac's filtered wideband output signal for the 4 DSD versions.

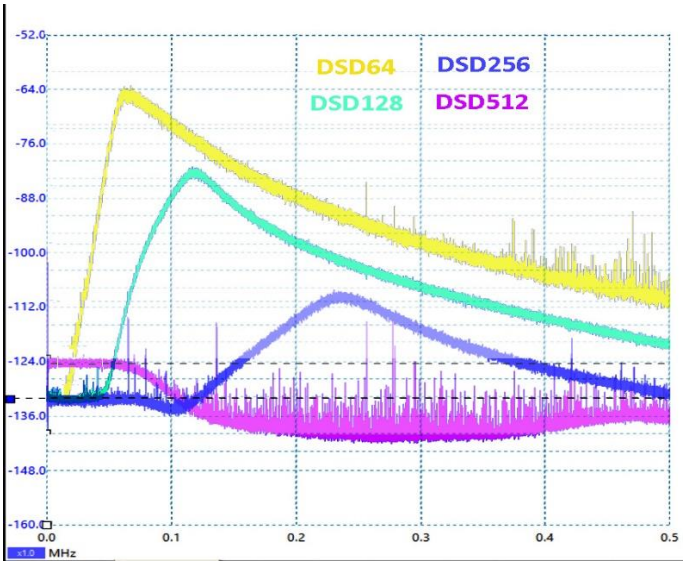

Fig 4, noise at the Firdac's output for various DSD versions

The DSD64 version is already slightly invading the 20Khz audio band, so DSD128 and especially DSD256 are giving clean spectra up to 20Khz and beyond.

Also obvious in Fig 4 is that DSD512 has a ca. 10dB higher noise level up to 20Khz. This could have various reasons, a less then optimal .wav to .dsf conversion from JRiver, or a crosstalk effect between clock and data somewhere in the digital hardware chain.
Changing the Amanero connection from a rather long 1.5 meter to a very short double isolated USB interlink did not bring any improvement.

Marcel produced a silent .dsf signal that was not SDM modulated, composed of a continuous 0101.. data flow, thereby enabling to just measure the analogue noise contribution from reconstruction filter plus shiftregister with its 3k01 resistors.
Result expressed in dB(A) for both signals, Silence and Silent Track are summarized in table 1.

	S/N Silence dB(A)	S/N Silent Track dB(A)
DSD128	111,7	105,3
DSD256	111,7	103,3
DSD512	111,7	95,7

Table 1, S/N for the various combinations

Table 1 shows a 105.3 dB(A) S/N for DSD128.
Compare this to Marcel's solid state Dac, where a figure of 103.9 dB(A) came out at first with the filter equipped with OP2134 op-amps, but where 108.5 dB(A) seemed possible when using 6k98 Firdac resistors instead of 32k4 versions, a somewhat modified filter and the OPA2210 instead of the OPA2134 for the reconstruction filter.
So, it seems that some 3dB(A) of the S/N gets lost, either in the JRiver .wav to .dsf conversion because it's a lossy process, but maybe also somewhere in the digital hardware processing.

When playing just Silence, excluding all noise contributed by SDM processing, Marcel's solid state Dac compares as follows to the shift register Firdac:
According to Table1, analogue noise for the shift register version is a fantastic 111.7 dB(A).
This was achieved with very low noise OPA2210 op-amps in the first stage and NE5532 for U5 and U6.
Marcel's original solid state Dac analogue section with OPA2134 measured 104.6dB(A), but after the above mentioned modifications it became 112.9 dB(A), comparable to the construction filter in the shift register version.

Conclusion:

With the proper .dsf files and high quality I2S conversion, a very good S/N can be achieved with Marcel's shift register Firdac.
Be aware that converting a PCM file into a .dsf file is potentially an inefficient and lossy process, depending on the used SDM model and calculation accuracy.
The original audio recording is most likely made with a high speed A/D, producing in most cases a multibit signal.
When this signal is converted into a full 16 bit PCM and thereafter by a conversion back into .dsf, something may get lost along the line.
The known disadvantage of 1 bit DSD is that it can't be processed in the digital domain without converting it to PCM and back, but unless you use some acoustic room correction filter that won't be an issue in most cases.

Epiloque:

After having been confronted with a big nonlogical drop of almost 10db in S/N when going from DSD128 to DSD512, the question rose what along the processing line was responsible for this deterioration.
That's why Marcel made a DSD512 file from a 44.1Khz Silent Track with his PWM8 SDM in high precision calculation.
Effect of this PWM8 algorithm is that the knee point where the modulated noise starts to rise is at ca 40Khz, comparable to a DSD128 made from 44.1Khz in Fig 4.

But in effect the S/N improved by 5.1dBA from 95.7dB(A) to 100.8 dB(A), just proving that Marcel's algorithm is more accurate than the one JRiver is using for this DSD version.

On the other hand, JRiver conversion is just reflecting the standard that is used for DSD processing, so it seems practical to avoid DSD512 in normal practice and to concentrate on DSD128 and DSD256 for the best possible S/N, at least when using the Amanero board.

Worth mentioning is that Marcel measured a S/N of 104.6 dB(A) with PWM8 with an even higher clockrate of 27Mhz but not through the Amanero and with well separated data and clock lines.
Clock and data lines on the Amanero's output connector are far from optimal sitting very close directly next to each other
So, it's not unlikely that there is quite a bit of crosstalk at this connection point, prohibiting to see the full potential in S/N of Marcel's Shiftregister Firdac.

With one Amanero channel even producing large spikes at DSD512, I was not impressed by this Dop to I2S solution that gave me the impression that DSD512 was in fact beyond its power.