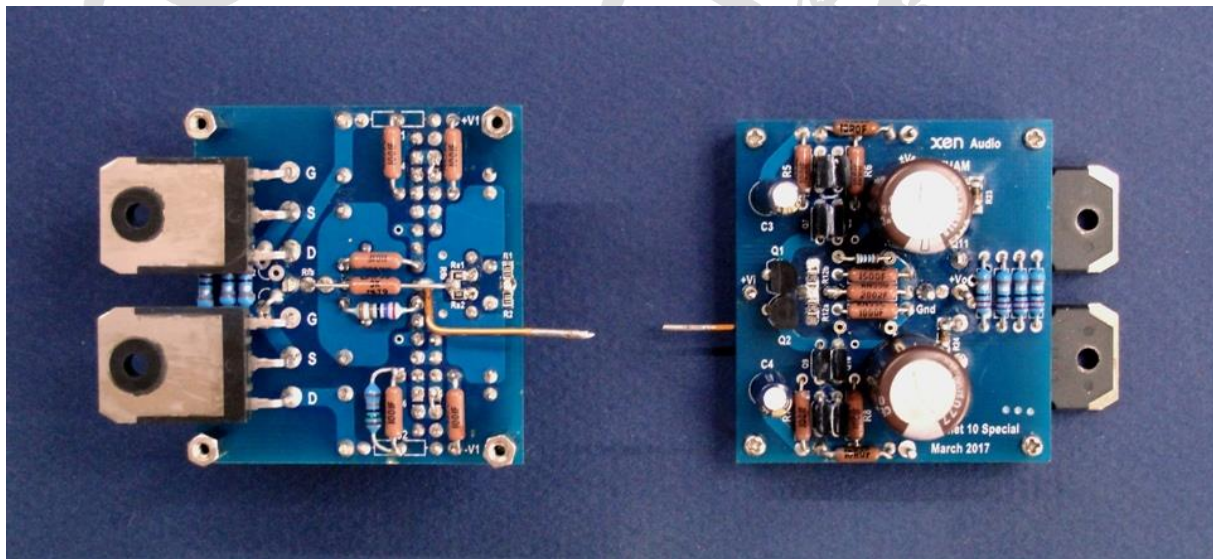


## UTHAiM, a fun Headphone Amplifier Project

XEN Audio

March 2017



### Background

Different from the DAO SE and Balanced DAO, which is a no-hold-back project driven only by performance, the UTHAiM (Universal Topology for Headphone Amplifier with Current Mirrors) is a fun project. With one single standard layout, it allows many variations with different component choices, the amount of negative feedback, different power supply schemes, etc. With the same PCB, you can, e.g., choose to use either MOSFETs or BJTs in the current mirror. You can also choose to use a 2-TR, 3-TR or 4-TR current mirror. You can apply zero global feedback, or varying degrees of negative loop feedback. You can vary the amount of source degeneration on each input JFETs, and play with degeneration on the output N-MOS or P-MOS. The only components with restricted choices are the output devices, as the PCB is designed for lateral-FET-compatible pin assignments. Even then, changing to vertical MOSFETs with degeneration is not impossible, just a bit fiddly.

The whole thing started with the discussion of the Pass HPA-1 topology [1], as disclosed by 6moon [2], and a schematics posted by juma at DIY Audio [3]. This was later realised in an example built by forum member needtubes, independently of the former [4]. In the same discussion, I also posted, just for fun, a schematics of an ALL-FET, Zero Global Feedback version of the above [5].

### Circuit Description

Essentially the circuit used a pair of complementary JFETs at the front end to swing signal currents of opposing polarities, which are then reflected back from both rails to the IV-resistor to generate the voltage gain required. This is followed by a pair of complementary lateral MOSFETs to generate sufficient current to drive the headphone. And if you so wish, you can close the feedback loop either before or after the lateral FET follower, or none at all.

So we can play with the choice of components for the three active functional blocks. For best performance, it is a no-brainer to go to the 2SK170BL/ 2SJ74BL input pair, preferably with a matched  $I_{dss}$  of  $> 8\text{mA}$ . If you prefer a higher voltage output (for 600R phones), then V grade is even better. But if you adapt the circuit intelligently, you can also use a pair of 2SK246Y/2SJ103Y with around 2mA

Idss. The price is 5x higher noise, 3x less bandwidth, and increased distortion. But it will still be a very listenable headamp even with ZGF. And you can always apply NFB to improve these measured performance figures.

As already mentioned, you can build a current mirror (CM) with 2~4 transistors, either MOSFETs or BJTs. All of the common CM configurations are well summarised in [6]. BJT mirrors generally have lower noise and require less voltage headroom, but have higher distortion due to the base current. I personally prefer the 4-FET CCM mirror for its lowest distortion. In any case, well-matched devices will always give you better performance than unmatched. I chose Zetex MOSFETs and BJTs in the E-line package because they are directly pin compatible and hence can just be swapped without layout changes. Also the flat E-line package is much better for thermal coupling than the standard TO92.

There are many source follower circuit around to get you sufficient drive current after the voltage gain stage. My own published circuits include the DAO TCS follower [7] and the LH0033 Sziklai [8]. There is also a self-biasing design from Wayne recently [9]. But I thought of using the lateral FET follower that I published recently in [10]. The fact that we already have 8mA bias current flowing from the top to bottom rail at the output branch makes for very easy bias of the laterals.

Why did I choose to use a pair of lateral FETs meant for power amps ? Apart from the known differences to the vertical FETs (much lower and more linear capacitances, but lower  $Y_{fs}$  and also lower  $V_{gs}$ ), lateral FETs has a negative temperature coefficient above the zero tempco point, which occurs at relatively low current. For the 2SK1058/2SJ162, this zero tempco is at around 100mA. That is ideal for Class A headphone amplifier output with a bias of 120 ~150mA, so that the tempco at bias is slightly negative. This means that the output devices will self-stabilise without resorting to using NTCs in the biasing circuit.

These TO3P devices also have a very low thermal resistance junction to case ( $0.8W/^{\circ}C$ ), making heat sinking and thermal tracking an easy task. Their transconductance at 150mA is around 0.3S, so that the output impedance is  $< 2R$  even without negative feedback. The N-FET has a somewhat higher  $Y_{fs}$  than the P-FET, which is why I included a degeneration resistor to make them more balanced. But if you are not too concerned about equal load current sharing, you can instead use R31 to reduce second harmonics, or you can even leave that out altogether and just bypass with a jumper. For second harmonics cancellation, depending on the  $V_{gs}$  of the laterals, you might need to connect R31 to the 2SJ162 instead of the 2SK1058. That is what the jumpers J31, J32 at the back of the PCBs are for. This output stage is really very simple, for the performance it offers.

Of course you can even skip the 2SJ162 altogether and just replace it with a 160R power resistor. The  $Z_{out}$  will go up to about 3R, and you will load the output device more. But if you are planning to use 25R phones anyhow, then an addition 160R is also no big deal. Your 2<sup>nd</sup> harmonics will certain goes up to add (artificial) "sweetness".

Incidentally, if you are planning to use this as a line amp, or to drive 600R loads, you might wish to experiment with a lower bias, say at 110mA. But it is important though not to go below the zero tempco bias. Alternatively, if you can find plenty of matched 2SK369V's, use 5 pairs of them in parallel as a standard N-JFET follower with  $\pm 12V$  rails. In that case you can skip R21, R22 altogether. Or even at add a TCS (Taylor Current Source) to lower even order harmonics and increase driving power further [11].

So you see, you can play with umpteen variations and decide for yourself which one you like best.

### **Suggested Setup Procedure**

A word of warning first -- you will only be able to enjoy all the fun with this project if you understand circuits and know what you are doing.

There are still suppliers around for pre-matched 2SK170BL/2SJ74BL, as well as 2SK1058/2SJ162. If you were to buy them pre-matched, you should ask the supplier to tell you the  $I_{dss}$  of the JFETs, and the  $V_{gs}$  of the MOSFETs at 150mA.

Knowing those values, you can calculate the values of R21,22 upfront.

$$R11 = (V_{gs\_1058} + R31 \times I_{bias}) / I_{dss\_JFETs}$$

$$R12 = (V_{gs\_162}) / I_{dss\_JFETs}$$

Choose the closest standard value, as you will have to trim them later on for DC offset.

Q3~10 are probably not available pre-matched. A simple matching circuit can be found in Appendix 4 if you wish to use MOSFETs. If you wish to use BJTs, you can simply measure  $h_{fe}$  using a suitable multimeter. Take note of the pin assignments of the Zetex BJTs.

It is best to set up the front end on its own. So it is advisable to leave out the lateral FETs first. Short the input to Gnd before powering up with a dual lab supply, with the current limit set at 25mA. Measure the voltage across R5,6,7,8 respectively. They should be almost identical and equal to  $(I_{dss\_JFET} \times 499)$ . If that is the case, measure the voltage across R11. If this voltage is negative, you should reduce the value of R6 by paralleling it with a trim resistor. If positive, you should trim R8 instead, until R11 is at 0V. Replace the trimmer with a fixed resistor at the back of the PCB. The front end is now trimmed for DC offset.

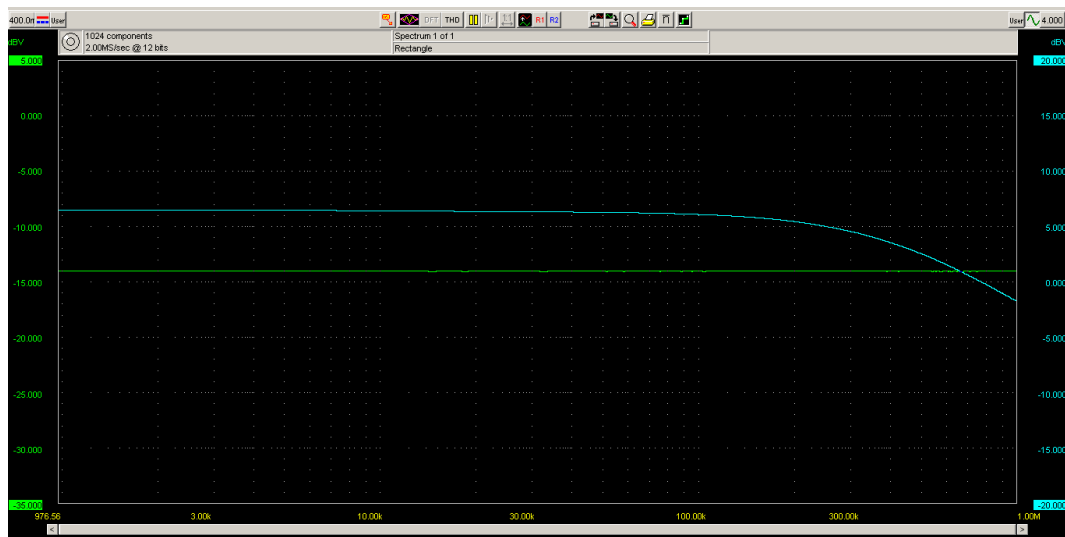
The lateral FETs can now be soldered and mounted onto heatsinks with Kerafols or similar. Readjust the lab supplier current limit to 0.25A, and power up again. The circuit should be drawing about 170mA. Measure the voltage at the output. If the output voltage is negative, you should reduce the value of R22 by paralleling it with a trim resistor. If positive, you should trim R21 instead, until the output DC is at 0V. Replace the trimmer with a fixed resistor (RN50 or equivalent) next to R21,22 on the top of the PCB (extra space & solder pads provided). The DC offset of the output is now also set.

## Measured Performance

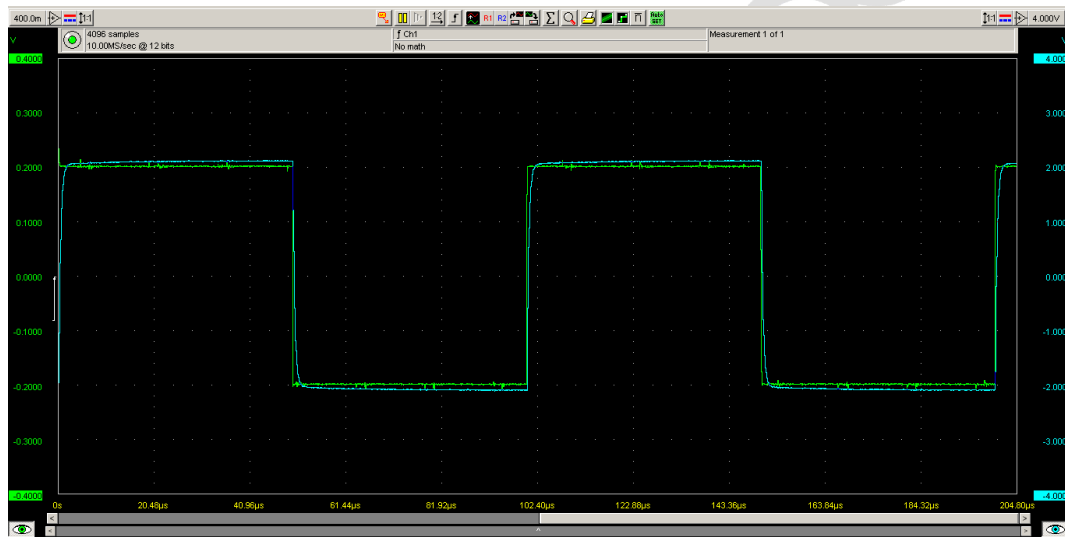
The followings are the measured performance of the All FET, ZGF version of the circuit, built on Vero boards.

Without any fine adjustments, the gain of Proto 1 was 10.18, and 10.37 for Proto 2 (or within 2%). A small resistor in parallel with R11 got this back to < 0.1%. The performance was essentially as simulated. -3dB bandwidth is 400kHz. DC offset stays within +/- 5mV in an hour after initial 5-minute warm up period. Bias was stable at ~150mA throughout.

On listening, I was expecting some noise because of the use of Zetex MOSFETs in the current mirrors. But there were none at all, not even on my most sensitive phones. This ZGF version has a similar sound to the XEN HAGS / DAO combination. It also has very tight, deep bass and has no issue whatsoever driving my AK701, known to be difficult for bass. Music is effortless. And I can understand why Charles Hansen like these lateral MOSFETs. The output stage is essentially the same as a Class AB power amp. So it is advisable to use some sort of headphone protection. The amplifier also functions all the way down to DC. So it is also wise to make sure the input signal is free of DC offset.



**Vero Proto 1** Frequency Response 0.2V Sine Wave at Input



**Vero Proto 1** 10kHz 0.2V Square Wave at Input